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Trends, Challenges, and Solutions in Advanced SoC Wafer Probe

FormFactor

MICROPROBE

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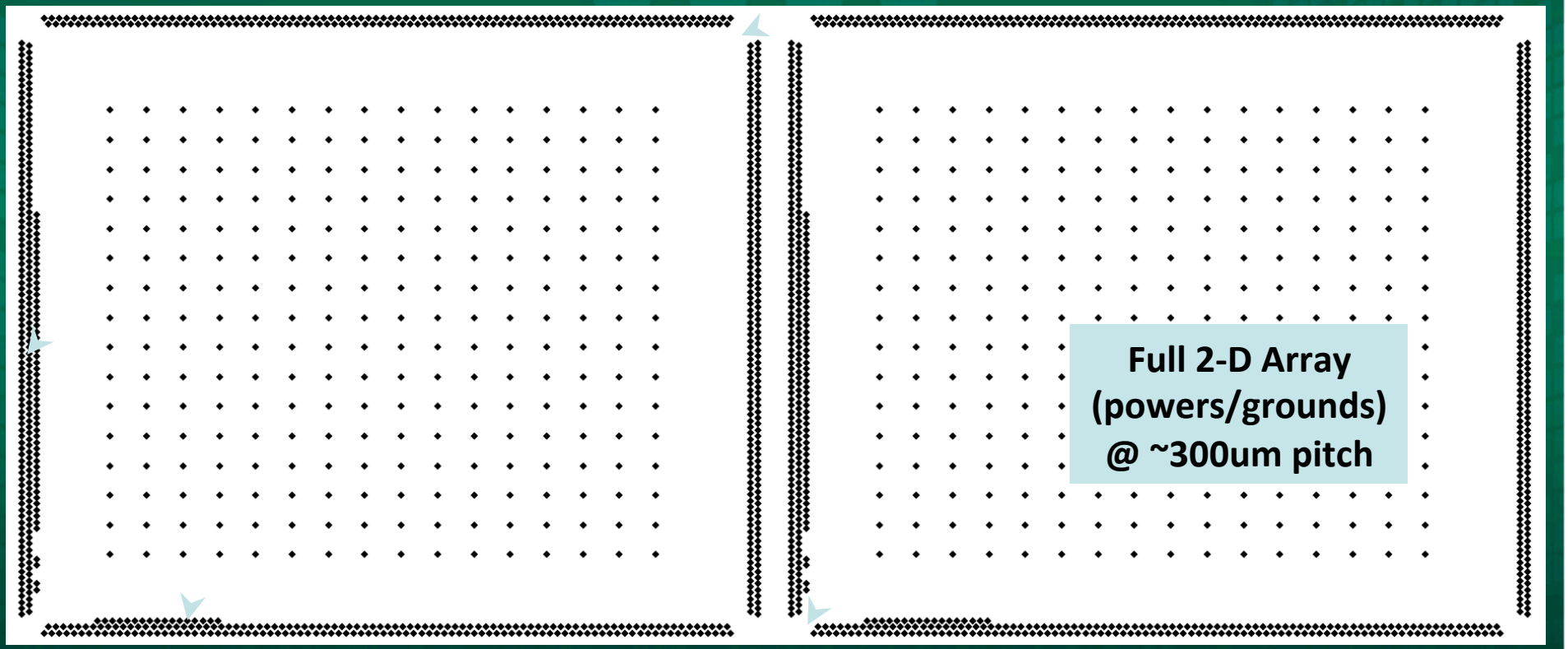
Outline/Summary

- Rapid recent adoption of advanced packaging
  - Copper pillar and C4 flipchip
- Driven by mobile cost and performance roadmaps
  - Customers relying on “more-than-Moore” advances
- Presents significant challenges for wafer test and probe
  - Layouts are fully-populated 2-D arrays at sub-100um pitches
  - Contacts are delicate structures made of new and diverse materials
  - Electrical performance (AC&DC) requirements continue to advance
  - Industry requires a “Moore-like” cost trajectory
- Solutions rely on a mixture of technologies from diverse areas
  - MEMS processing, materials science, signal integrity, etc.

Contemporary Packaging Layouts Demand a Vertical Probe Architecture

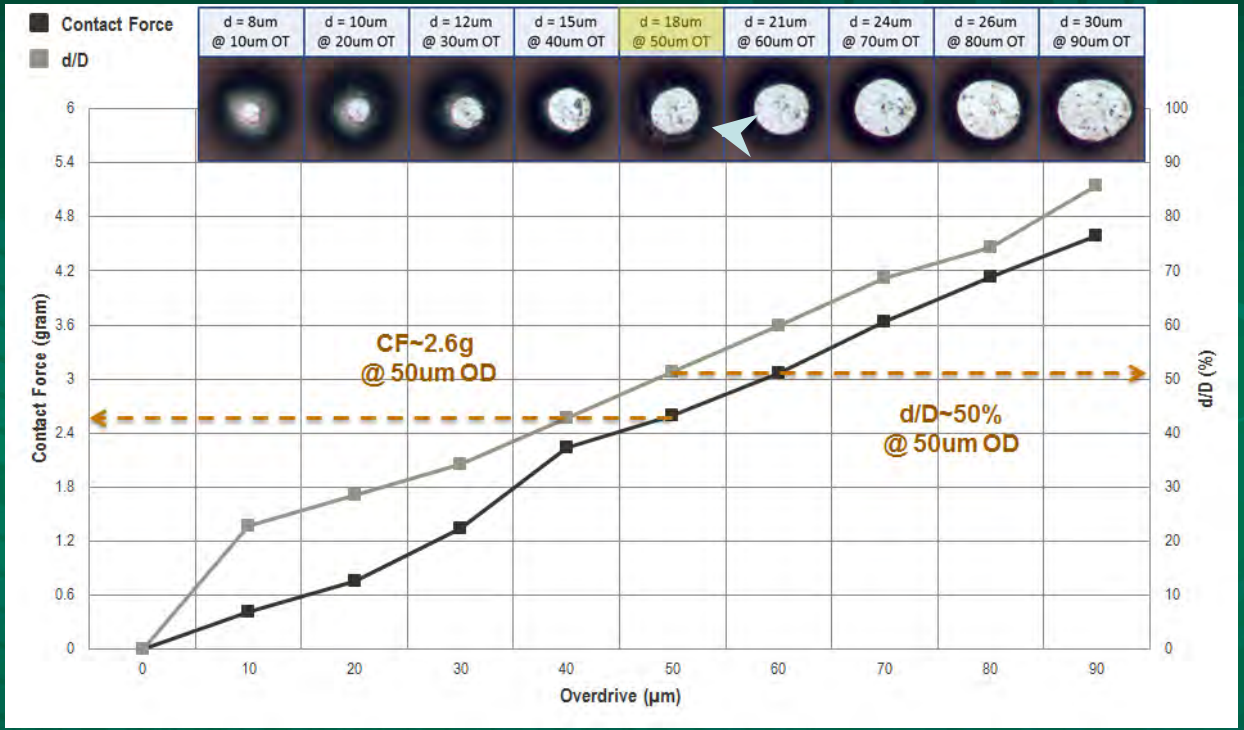
3 Rows @ ~80um min pitch
(some 4-row designs in '13)

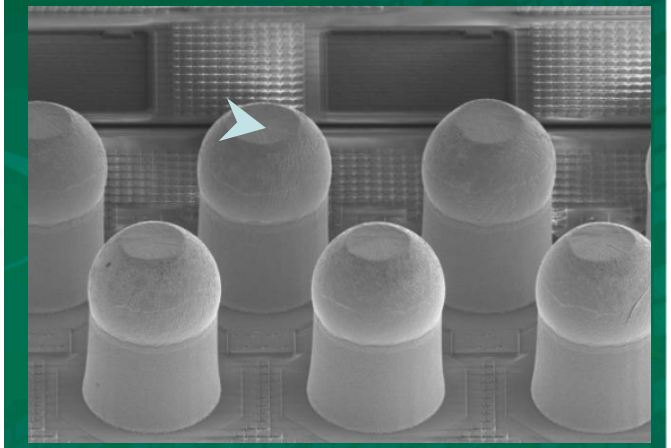
Minimal (~250um)
corner keepouts



Example – x2 Card for 80um Copper Pillar Device

These 2-D Layouts Populated With Structures That Require Low Probe Forces





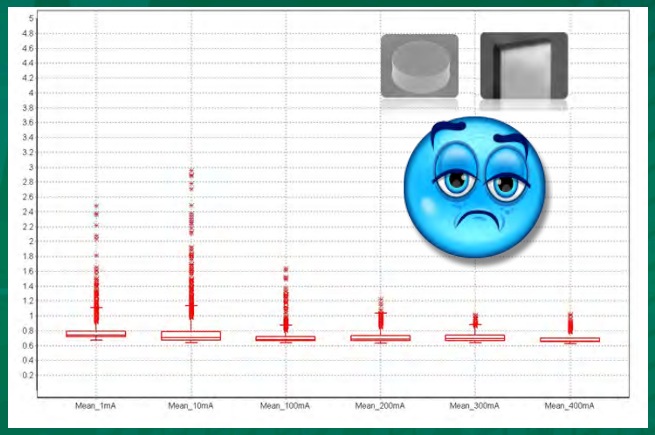
- Typical SnAg damage (d) requirement <50% of pillar diameter (D)
  - Additional requirements on probe mark topology (notching, smearing, etc.)
  - Imposed by assembly constraints (reliability)
    - Met with probe forces of 2-3g for 30um < D < 40um

At Low Force, Probe Material and Geometry Optimization Required for Stable Electrical Contact

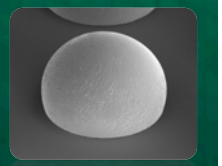
MEMS Probe #1

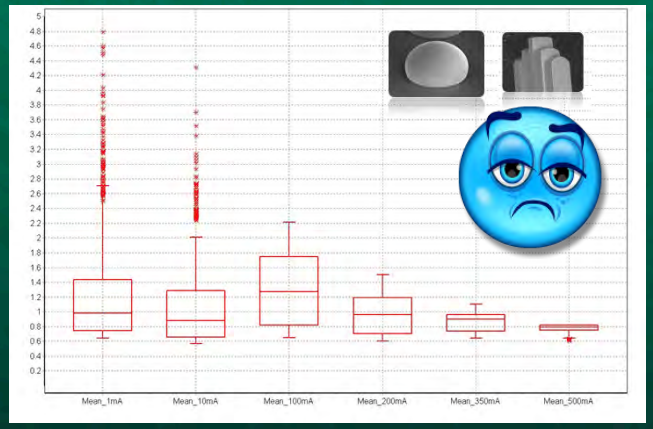
MEMS Probe #2

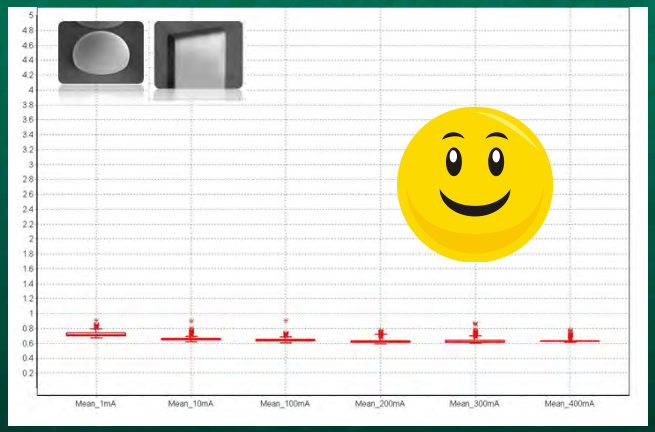
Bare Copper Pillar



SnAg Bump

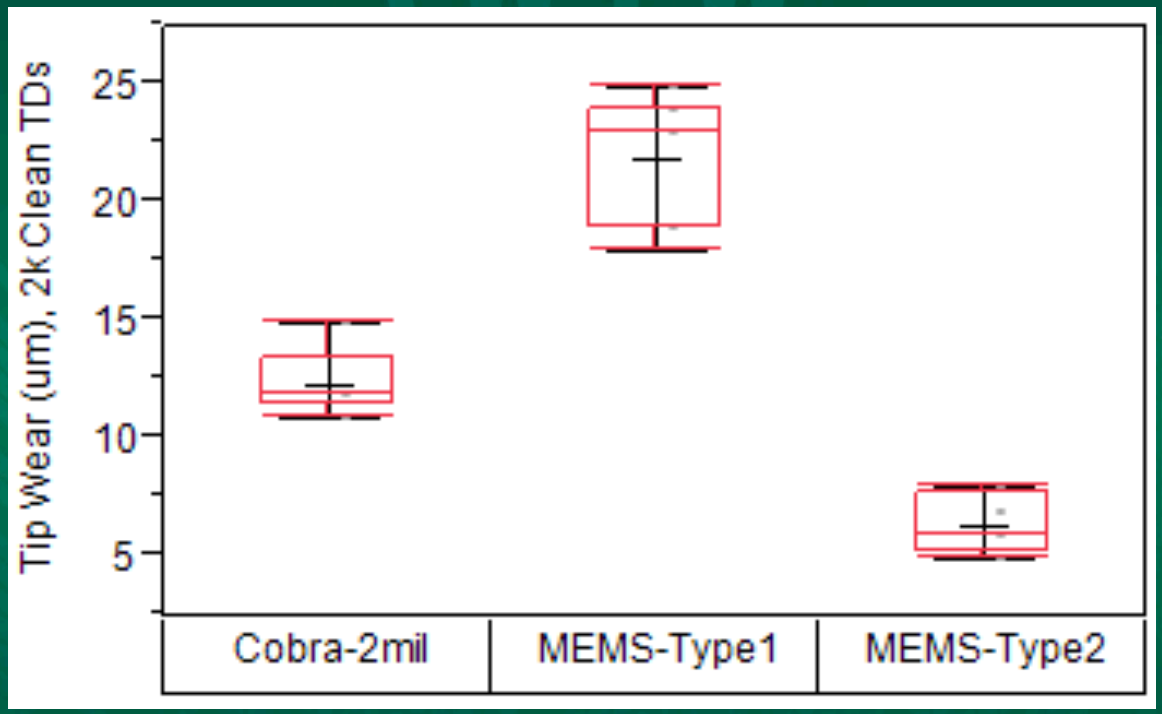






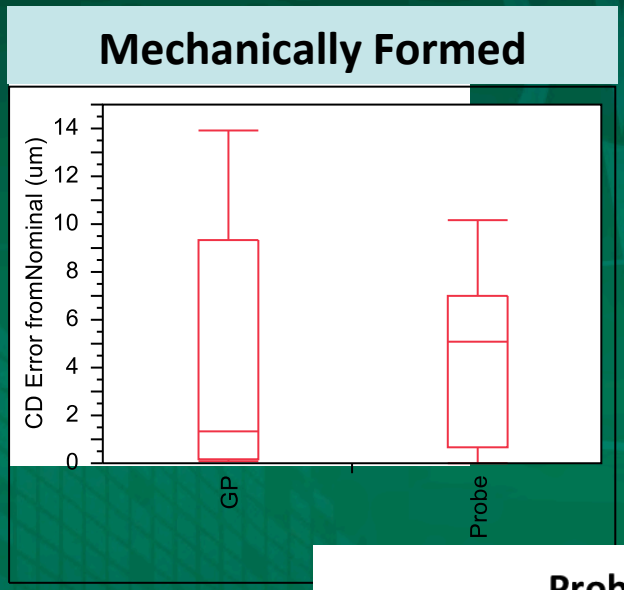
Source: Wittig et al, SWTW 2011

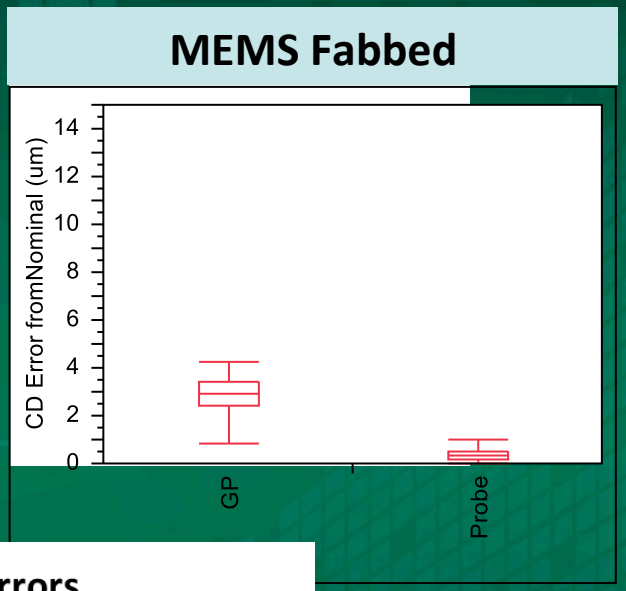
Overall Cost Also Strongly Influenced by Probe Material and Geometry



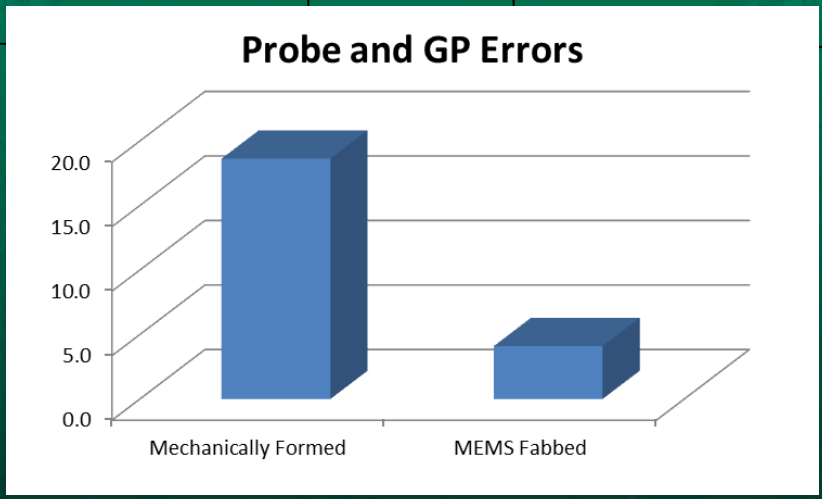
- 4x difference in wear/lifetime for different probes
  - Same (standard HVM) cleaning recipe used

Dimensional Control Improved With MEMS-Based Fabrication Processes

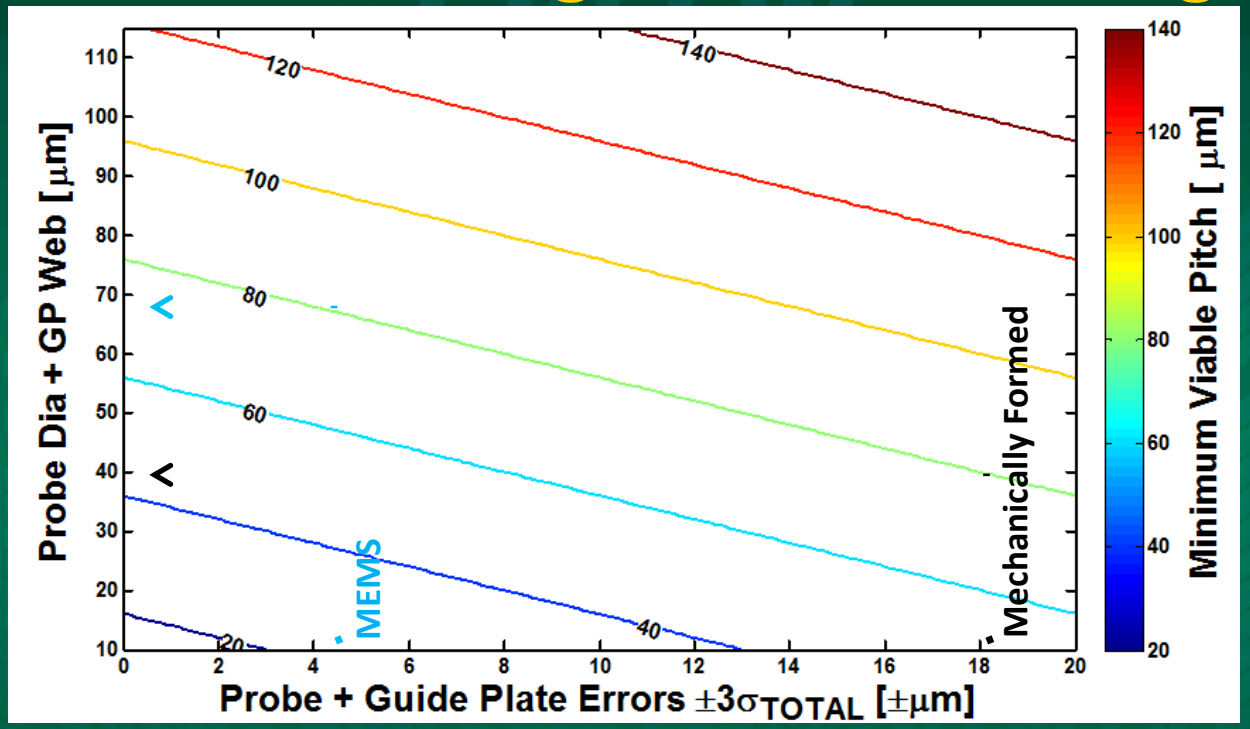




- Raw "as-fabbed" distributions
- Indicative of natural process capability

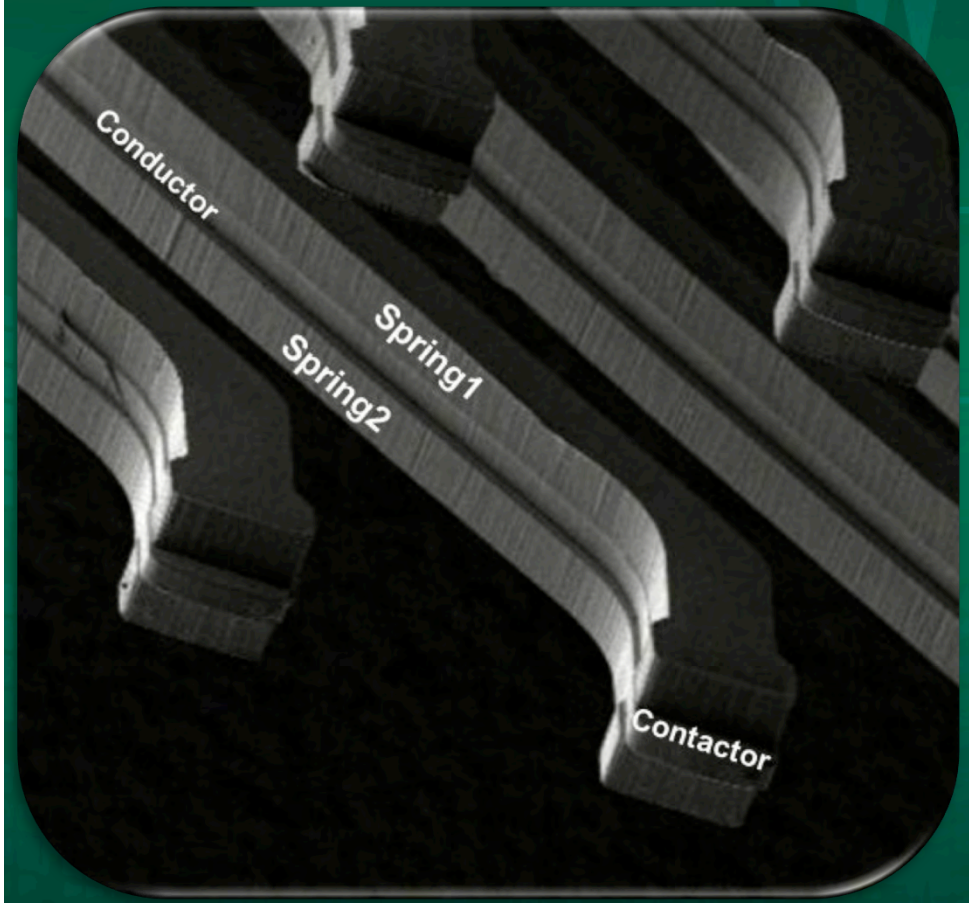


For Sub-100um Pitches, MEMS-based Dimensional Control Offers Significant Advantages



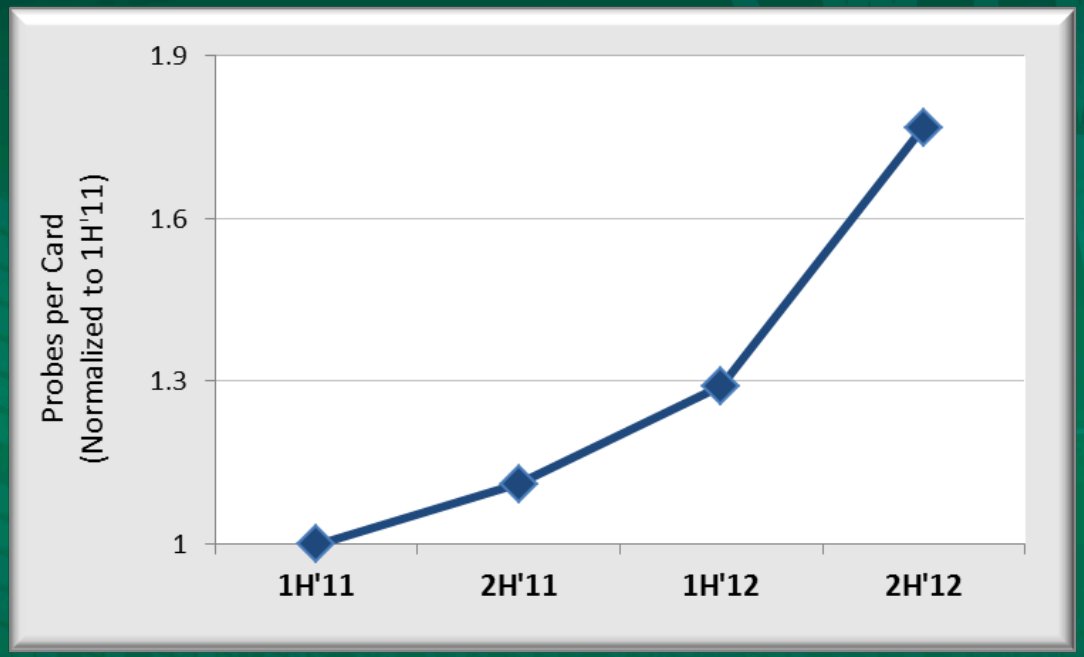
- Reduction in as-produced dimensional errors can be used in different ways:
  - Larger probe for a given design pitch - for 80um example above, Δ=25um
    - Better electrical performance (current, impedance) and longer lifetime
  - Smaller minimum-viable pitch for a given probe
    - Improved design coverage and extendibility
  - Higher probe/GP component yield for cost reduction

Composite MEMS Probes Enable Optimization of Mechanical and Electrical Characteristics



- Different materials, in different locations, doing different jobs
  - Analogous approach to composite design in other fields (eg, aerospace)
- Fabricated with semiconductor/MEMS lithography & direct-write technologies
  - Dimensional control ~5x improved over mechanical forming
  - Short cycle time customization

And On Top of It All, There are More and More of These Probes in Each Card



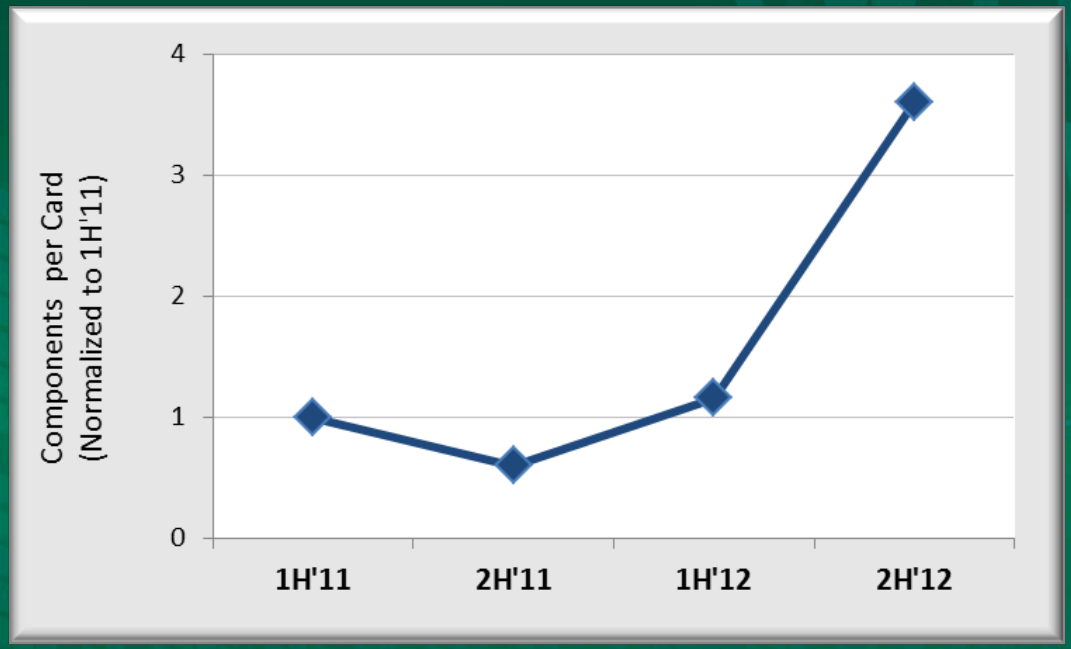
Source: Internal MP/FFI MEMS Shipment Data

Implications

- Card will sample "tails" of probe+guideplate distributions
  - Cpk > 1.33 processes req'd
  - Or, cost and leadtime suffer
- Quality and process control systems become critical

- Two primary drivers/causes (roughly equal influences)
  1. Increased parallelism – more DUTs for test cost reduction
  2. Increased probes per DUT – more test content and complexity per DUT

Component Count Increase a Reflection of Complexity-Per-DUT Increase



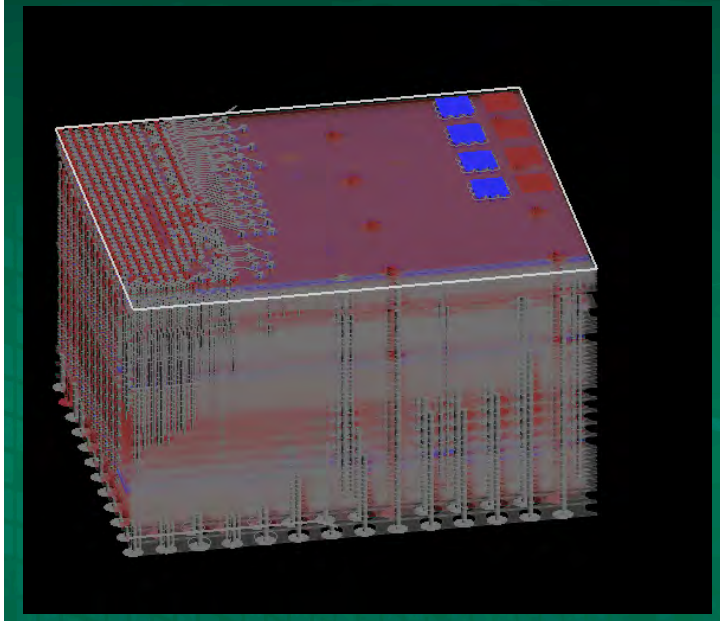
Source: Internal MP/FFI MEMS Shipment Data

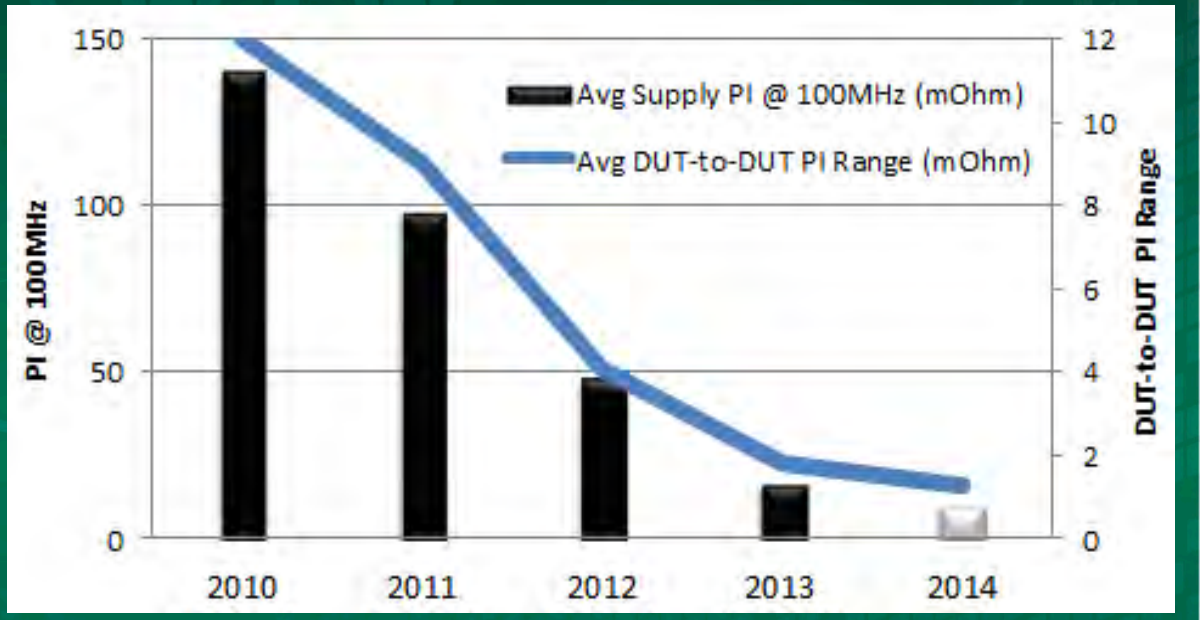
Implications

- Increase in PCB complexity – design, validation, and fab
  - Simulation and validation tools/ processes key to error reduction (leadtime/OTD)
- Deploying PCB assembly+test technologies from other areas
  - Rapid advancement of standard SoC probecard PCB processes

- Primarily driven by increase in number and performance of critical power supplies
  - Particularly evident in low-power multi-core architectures

Impedance Performance of Power Supplies Critical to Yield of Low-Power Mobile Devices





- AC impedance of critical power supplies limiting wafer sort yield
  - Full 3-D simulation of probe-to-tester interconnect standard validation
- Continued advances in interconnect (MLC/MLO) required
  - Wired space transformers (and low-end MLCs) not viable in these apps

Summary – Trends, Challenges, and Solutions

- Trends and Challenges are directionally familiar
- But, these familiar directions are rapidly accelerating
  - 2-D Grid Array pitches below 100um
  - Bump/pad materials and structures demanding <2-3g of probe force
  - Continued improvement in contact stability performance
  - AC impedance reduction of 10x in 3 years
  - Exploding probe (2x in 2 years) and component (4x in 2 years) counts
  - Continuing cost and leadtime reductions
- Solutions encompass a spectrum of technologies and processes
  - Composite MEMS structures
  - Sophisticated electrical design, validation, and test tools+processes
  - Semiconductor-inspired process control and quality systems