IEEE SW Test Workshop
Semiconductor Wafer Test Workshop
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When Brick Wall is not the best, PART II (A Touch Down Optimization Study)

Al Wegleitner
Texas Instruments

Tommie Berry
FormFactor

Overview
Touch Down Optimization(TDO)

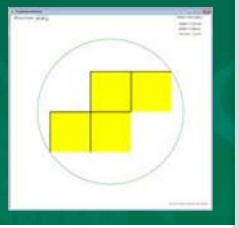
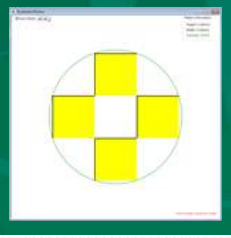
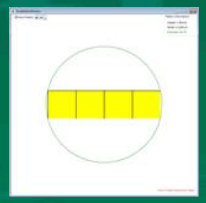
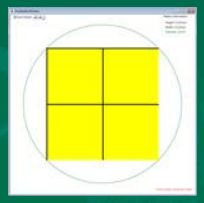
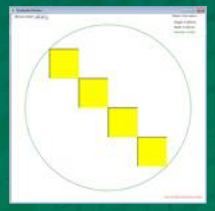
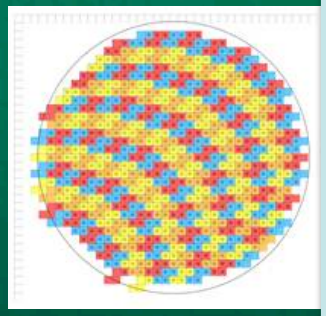
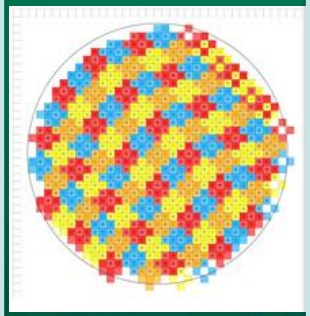
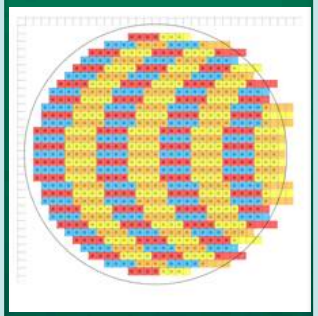
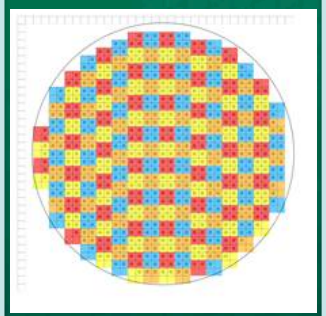
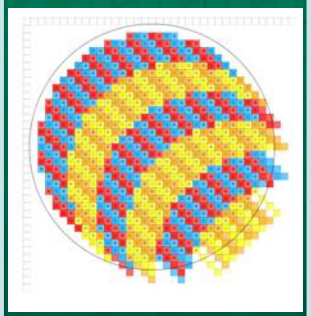
- Examples show why site layout is not obvious
- Choosing the site count and probe head layout
- Solid Array (Brick-Wall) is not always better
- Crosstalk issues
- Power (di/dt) noise issues
- Multi-Layer-Ceramic (MLC) routing issues
- Sharing tester resources to increase parallelism

TDO Comparison Study

- **Test Cell Time ($) for 1 wafer depends on**
  - Test Time for each TD
  - Average Prober Move Time
  - Touchdown Count Per Wafer
- **Optimize the following**
  - Parallelism & Probe Head Arrangement
  - What is the best stepping pattern
    - Minimize TD Counts
    - Minimize Prober Total Stepping Distance
- **We will look at 3 designs as examples**

Design #1, 4 DUTS

200mm wafer
3.5mm edge keepout
6x6mm die step
749 die per wafer

	200 TDs	201 TDs	202 TDs	203 TDs	208 TDs
Efficiency →	93.6%	93%	92.7%	92%	90%
Probe Head Configuration					
TD Pattern					

4% Improvement Opportunity

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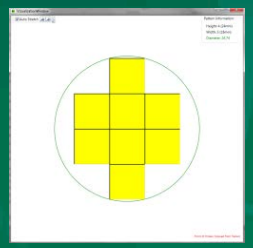
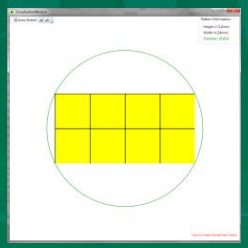
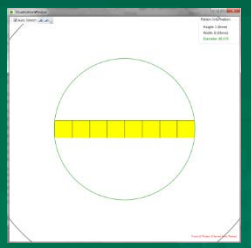
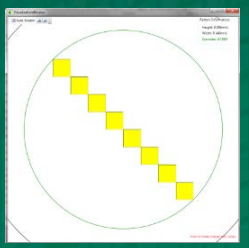
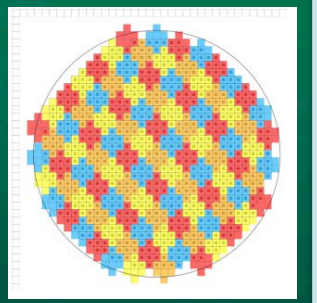
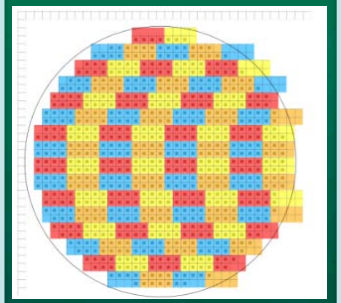
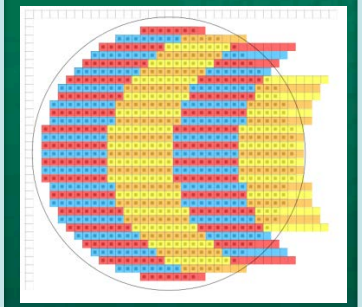
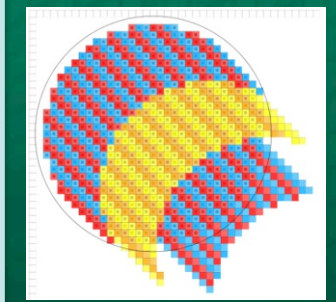
Design #1, 8 DUTS

200mm wafer
3.5mm edge keepout
6x6mm die step
749 die per wafer

	104 TDs	105 TDs	106 TDs	113 TDs
Efficiency	90%	89.0%	88%	83%
Probe Head Configuration				
TD Pattern		202 TDs 		

7% Improvement Opportunity

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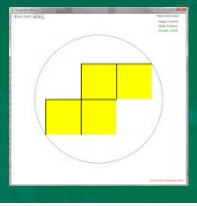
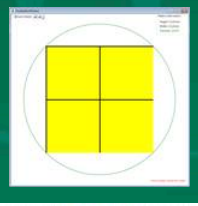
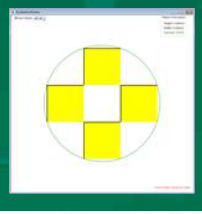
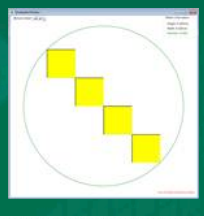
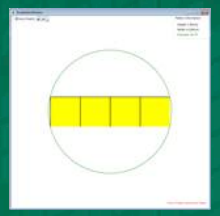
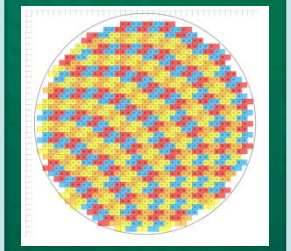
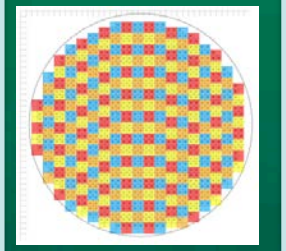
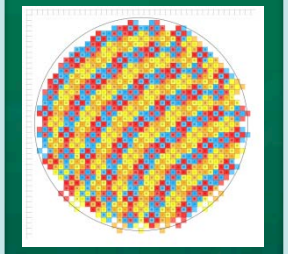
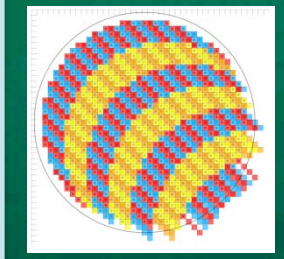
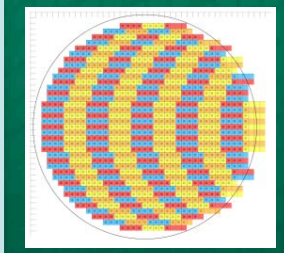
Design #2, 4 DUTS

200mm wafer
3.5mm edge keepout
6x6mm die step
1085 die per wafer

	288 TDs	290 TDs	291 TDs	291 TDs	292 TDs
Efficiency →	94%	93.5%	93%	93%	92.9%
Probe Head Configuration					
TD Pattern					

← 1% Improvement Opportunity ←

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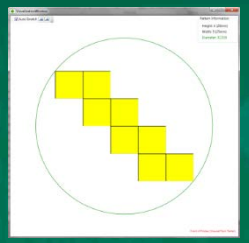
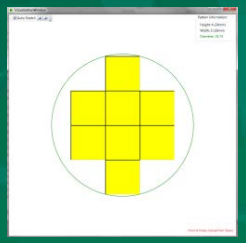
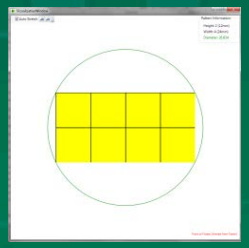
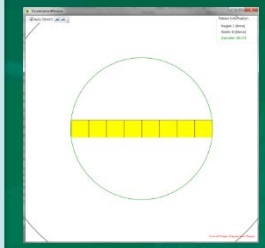
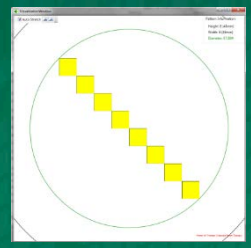
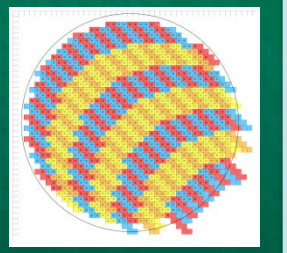
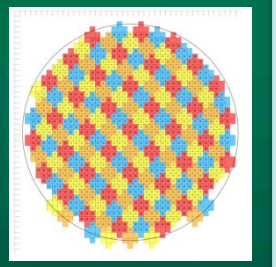
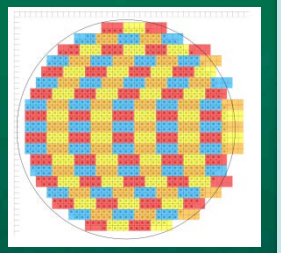
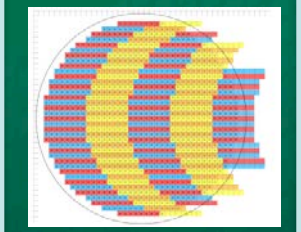
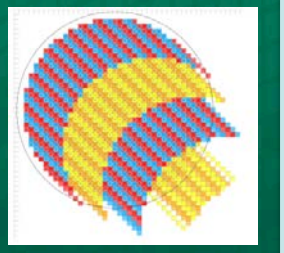
Design #2, 8 DUTS

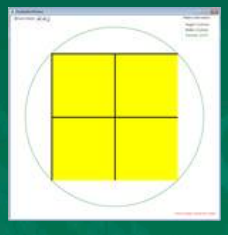
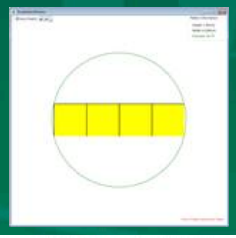
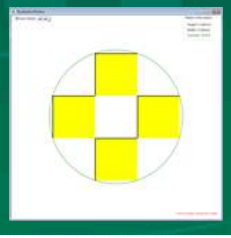
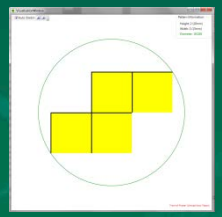
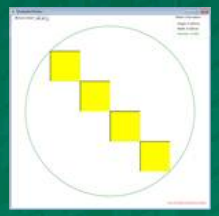
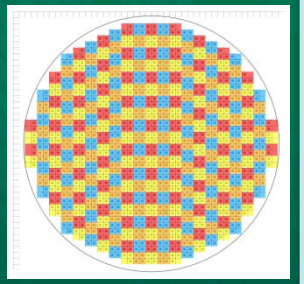
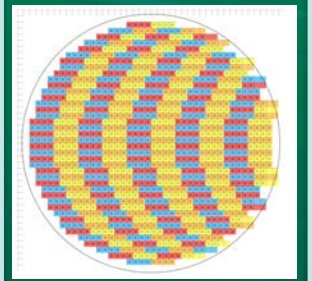
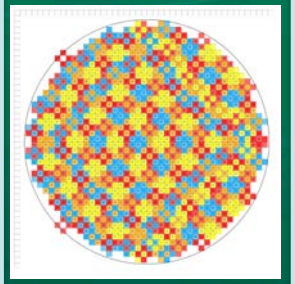
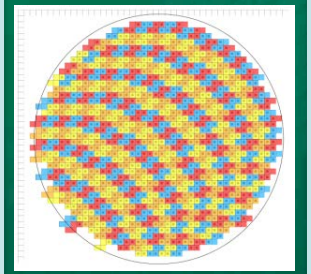
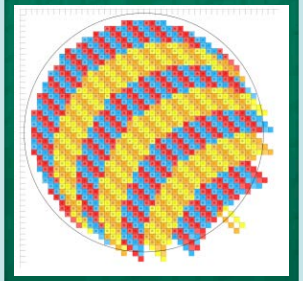
200mm wafer
3.5mm edge keepout
6x6mm die step
1085 die per wafer

	150 TDs	150 TDs	151 TDs	155 TDs	162 TDs
Efficiency →	90.4%	90.4 %	89.8%	87.5%	83.7%
Probe Head Configuration					
TD Pattern					

← 7% Improvement Opportunity ←

Design #3, 4 DUTS

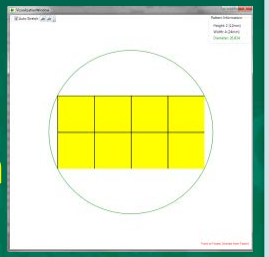
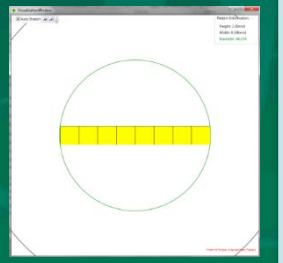
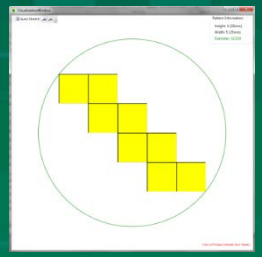
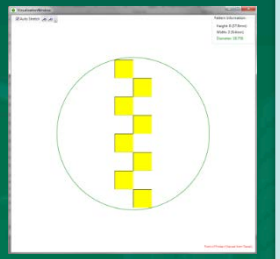
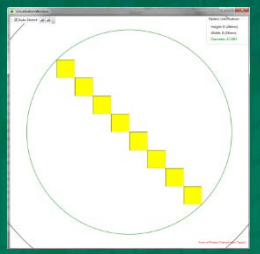
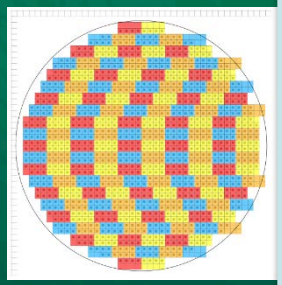
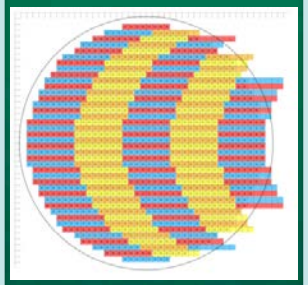
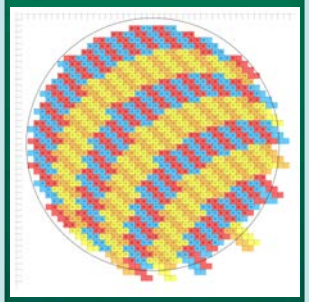
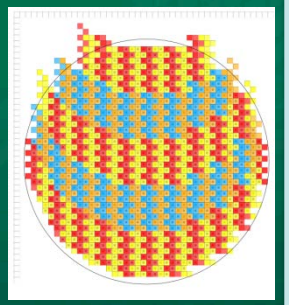
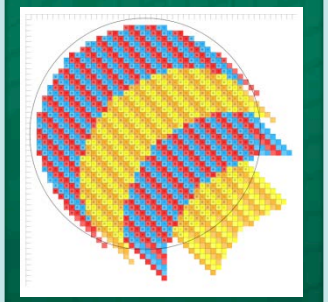
200mm wafer
3.5mm edge keepout
6x6mm die step
1240 die per wafer

Efficiency	320 TDs 96.9%	320 TDs 96.9%	324 TDs 95.7%	326 TDs 95.1%	331 TDs 93.7%
Probe Head Configuration					
TD Pattern					

3% Improvement Opportunity

Design #3, 8 DUTS

200mm wafer
3.5mm edge keepout
6x6mm die step
1240 die per wafer

	164 TDs	166 TDs	170 TDs	171 TDs	184 TDs
Efficiency →	94.5%	93.4%	91.1%	90.6%	84%
Probe Head Configuration					
TD Pattern					

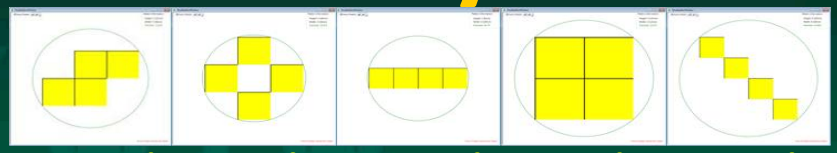
← 10% Improvement Opportunity ←

SWTW

June 9 - 12, 2013
IEEE Workshop

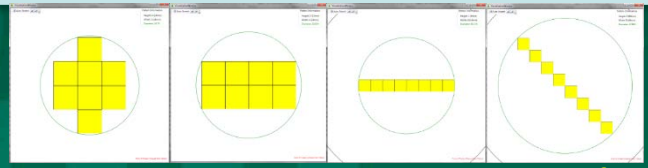
TDO Summary

- Design #1, 749 DPW x4



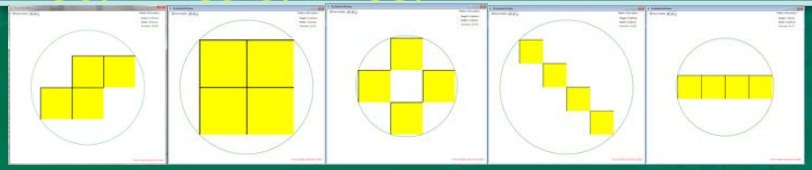
93.6% 93% 92.7% 92% 90%

- Design #1, 749 DPW x8



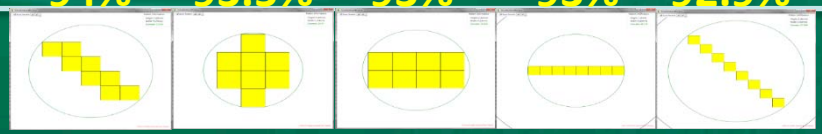
90% 89.0% 88% 83%

- Design #2, 1085 DPW x4



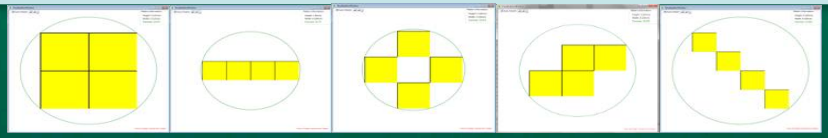
94% 93.5% 93% 93% 92.9%

- Design #2, 1085 DPW x8



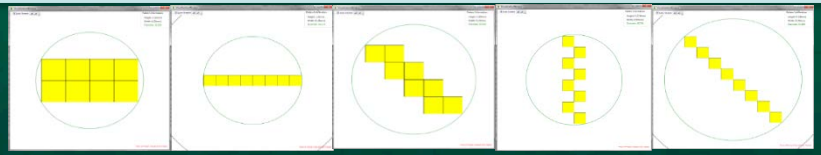
90.4% 90.4% 89.8% 87.5% 83.7%

- Design #3, 1240 DPW x4



96.9% 96.9% 95.7% 95.1% 93.7%

- Design #3, 1240 DPW x8



94.5% 93.4% 91.1% 90.6% 84%

New TDO tool on 13 TI Designs

Original TI Data			Percent Effeciency Improvement by using the new TDO tool					
Device TWSETUP	NUM SITES	DIE per wafer	Solid	SR	SC	SRSC	Matrix	TD Count improvement
#1	2	395	2.8%	2.8%	4.2%	1.4%	-10.0%	4.3%
#2	2	800	3.0%	2.3%	3.0%	2.1%	-15.2%	3.1%
#3	2	1077	3.4%	1.0%	3.4%	1.0%	-13.8%	3.4%
#4	4	818	1.3%	1.3%	0.0%	-1.7%	-14.4%	1.4%
#5	4	846	4.7%	4.3%	3.4%	-0.1%	-12.9%	4.4%
#6	4	2350	1.4%	-0.2%	0.8%	-1.1%	-18.1%	1.5%
#7	8	975	3.4%	1.3%	2.0%	-4.9%	-13.7%	3.6%
#8	8	1566	1.3%	-0.4%	0.4%	-2.5%	-13.8%	1.4%
#9	8	5353	9.0%	8.3%	8.5%	6.0%	5.6%	9.3%
#10	16	3358	13.8%	11.5%	12.7%	9.2%	1.3%	5.8%
#11	16	5252	1.9%	0.8%	0.0%	-2.1%	-12.8%	2.0%
#12	32	930	6.6%	4.2%	4.2%	-3.8%	6.6%	7.9%
#13	32	1065	9.7%	0.0%	0.0%	-6.3%	7.6%	11.4%
Average New TDO Tool Improvements in Efficency --->			**4.8%**	**2.9%**	**3.3%**	**-0.2%**	**-8.0%**	**4.6%**

Crosstalk issues

- Routing out from a 0.5mm or 0.8mm Ball Grid Array is a huge challenge for just one DUT.
- Solid Brick for even 2x2 arrays can double the ceramic and PCB layer counts.
- Routing very fine pitch lines through a brick wall will not allow the layout to use best practice cross talk routing rules.

Power (di/dt) noise issues

- Achieving low Mutual Loop Inductance on high di/dt supplies can be impossible without skip row, skip column or a matrix design.
- Skipping allows bigger planes with less holes.
- Also leaves more room for highly needed caps.
- Brick-Wall is not always the best solution.

Routing Issues

- Getting traces out from the center of a large BGA can be impossible with solid arrays.
- Power Plane Routing is much better with skip row/skip column
- Layer count is limited on MLC depending on many factors but using a solid array for probe cards instead of skip can drive the required layer count out of reach.
- High layer count MLC is very expensive.

Sharing tester resources To Increase Parallelism

- **Many customers are adding circuits to increase parallelism**
- **Tester Resource Enhancement (TRE) can be:**
  - Simple Shared Drivers
  - Resistor Protected Shared Drivers
  - Simple Shared Power Supplies
  - Relay Shared Power Supplies
- **All these options require room for circuits**
- **With Solid Arrays, this is very limited.**

Conclusions

- FormFactor has new advanced TDO (Touch Down Optimization) software that can be used on new designs to find the lowest TD for a given wafer pattern
- In many cases, a "special" pattern can do better than brick wall or simple rectangular or diagonal patterns
- Diagonal patterns as they get larger (esp for x8 and >x8) will generally not do as well as more compact layout patterns
- There is no general rule for which pattern will be the best – e.g. – the statement that brickwall is always the best is not correct. For the lowest # of TDs per wafer – an analysis should be done on each new wafer pattern and each parallelism.
- Crosstalk, di/dt Power Issues, layer counts and routing often force skip anyway. This tool allows you have the best of all worlds.