

28nm Mobile SoC Copper Pillar Probing Study



Jose Horas (Intel Mobile Communications)



MICROPROBE

Amy Leong (MicroProbe)



Darko Hulic (Nikad)



IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

June 10 - 13, 2012 | San Diego, California

Overview

- **Introduction to IMC**
- **Copper Pillar Implementation at IMC**
- **Low-force Vertical Probing Qualification**
 - Probe mark characterization
 - Contact resistance stability
 - Test reproducibility
 - Probing - Packaging interaction (coplanarity)
- **Future Work**
 - Probing - Silicon interaction (PoAA)
 - Hardware lifetime
- **Conclusion**

Introduction to IMC

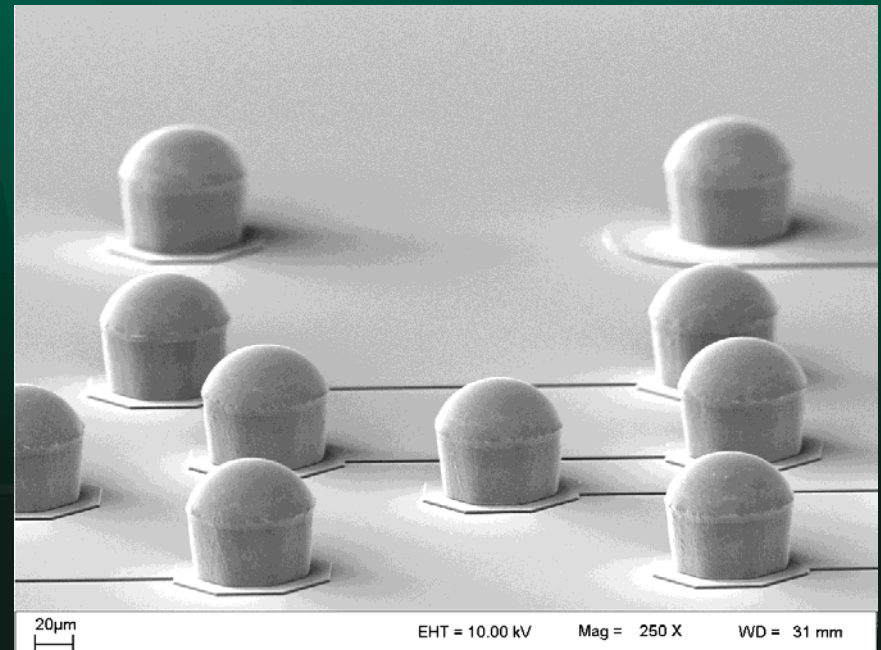
- **Intel Mobile Communications (within Intel MCG) develops products and solutions for mobile communications**
 - 2G/3G single-chip, 3G and 4G slim modem and RF solutions
- **4000 employees worldwide, 1700 work in Germany**



Copper Pillar (CuP) Advantages

- IMC roadmap includes Cu pillar bumps with lead-free SnAg caps
- CuP delivers several advantages compared to SnAg bumps:
 - Lower than 150 μm pitch
 - Lower substrate costs due to relaxed design rules and no solder-on-pad
 - Lower packaging cost thanks to easier Molded Underfill process
 - Better current carrying capacity
 - Better thermal performance
- Allows analogous probing and assembly processes as SnAg bumps

| Typical Value | CuP w/ SnAg caps | SnAg Solder bumps |
|---------------|-------------------|-------------------------|
| Pitch | 120 μm | 150 μm |
| Diameter | 70 μm | 100 - 110 μm |
| Height | 75 μm | 75 - 80 μm |



* B. Ebersberger, C. Lee, "Cu Pillar Bumps as a Lead-Free Drop-in Replacement for Solder-Bumped, Flip-Chip Interconnects", *Proc 58th Electronic Components and Technology Conf.*, Lake Buena Vista, FL, May 27 – May 30, 2008, pp. 59-66.

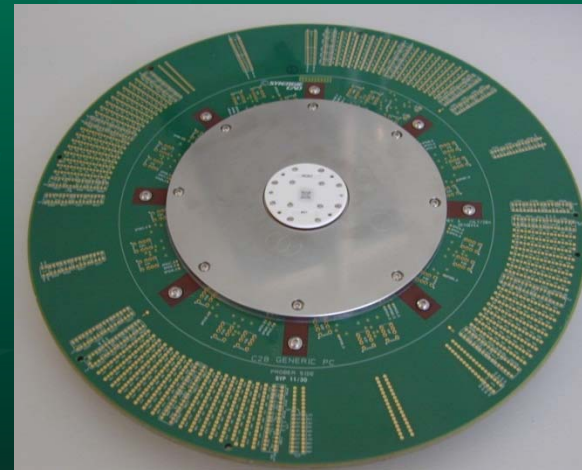
CuP Probing Solution Qualification Test Set-up

- **Objective**

- Characterize low-force vertical probe technology for fine-pitch full grid-array CuP application

- **IMC Device**

- 28nm Mobile SoC Test Chip
- Copper pillars with SnAg caps
- Minimum pitch of 120um



MicroProbe Low-force Apollo™ Card

- **MicroProbe Probe Card**

- Apollo™ product
- 2.5mil vertical probe
- Low-force optimized: 2.5-4 gram/probe @ production OD

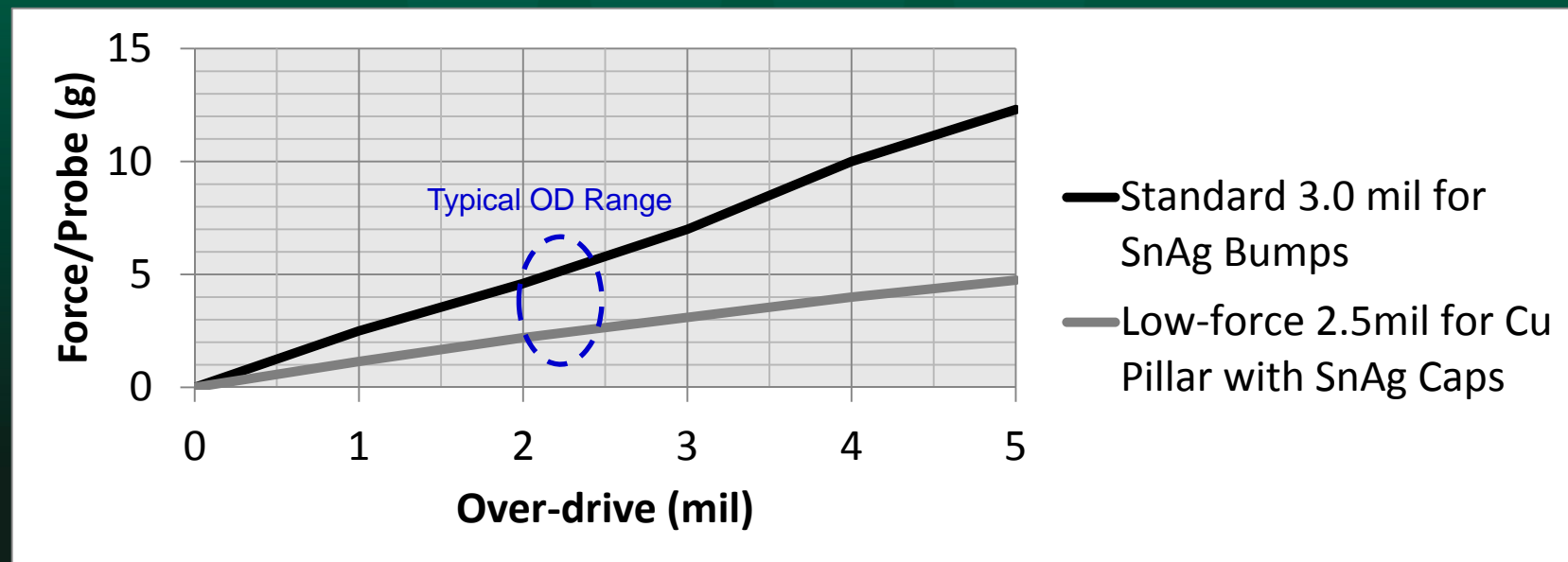
Low-force Apollo™ Probe Card

Key Evaluation Criteria

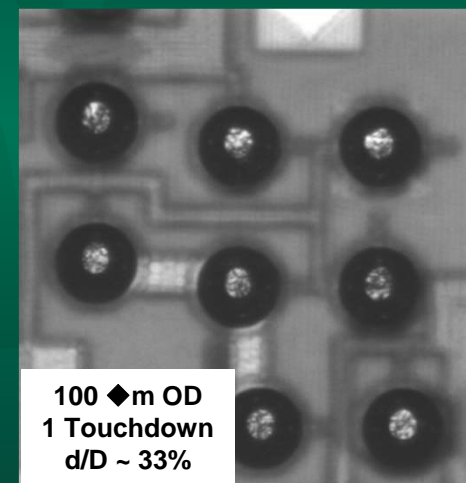
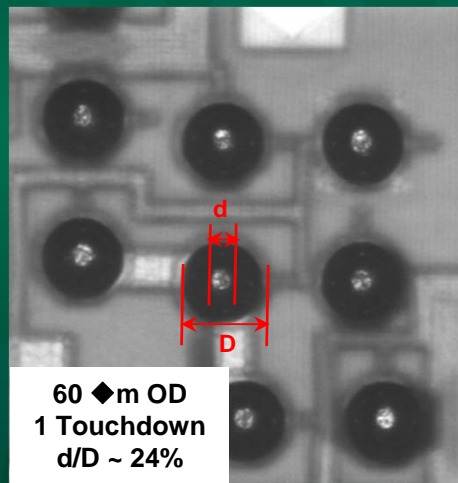
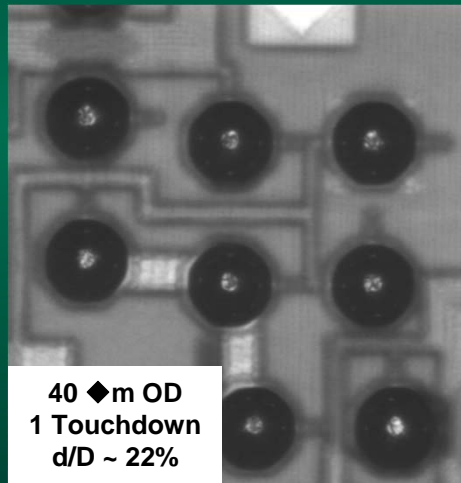
- **Key Evaluation Criteria**
 - Mechanical
 - Probe force vs. overtravel
 - Probe mark quality vs. overtravel
 - Probing over Active Area (PoAA) reliability
 - Production life-time study
 - Electrical
 - Contact resistance (Cres) stability
 - On-line cleaning recipe
 - Test (binning) reproducibility
 - Probe-Packaging Interaction
 - Pillars co-planarity

Probe Force: Low-force Vertical Probes for Thin SnAg Caps

- Apollo™ low-force probes were used to minimize probe damage to thin SnAg caps on Cu Pillar
- At an over-drive of 2 mil, low-force 2.5mil probe offers 50% probe force reduction compared to a 3.0mil probe typically used for SnAg bumps

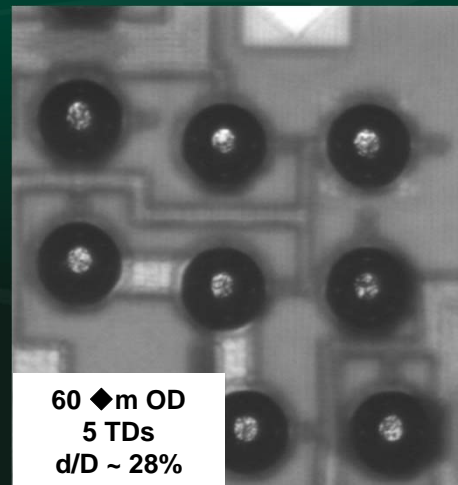


Probe Mark: Low-force Probes Satisfy Probe Mark Quality Requirement



Probe Mark Guideline

$d/D < 50\%$ to ensure packaging reliability

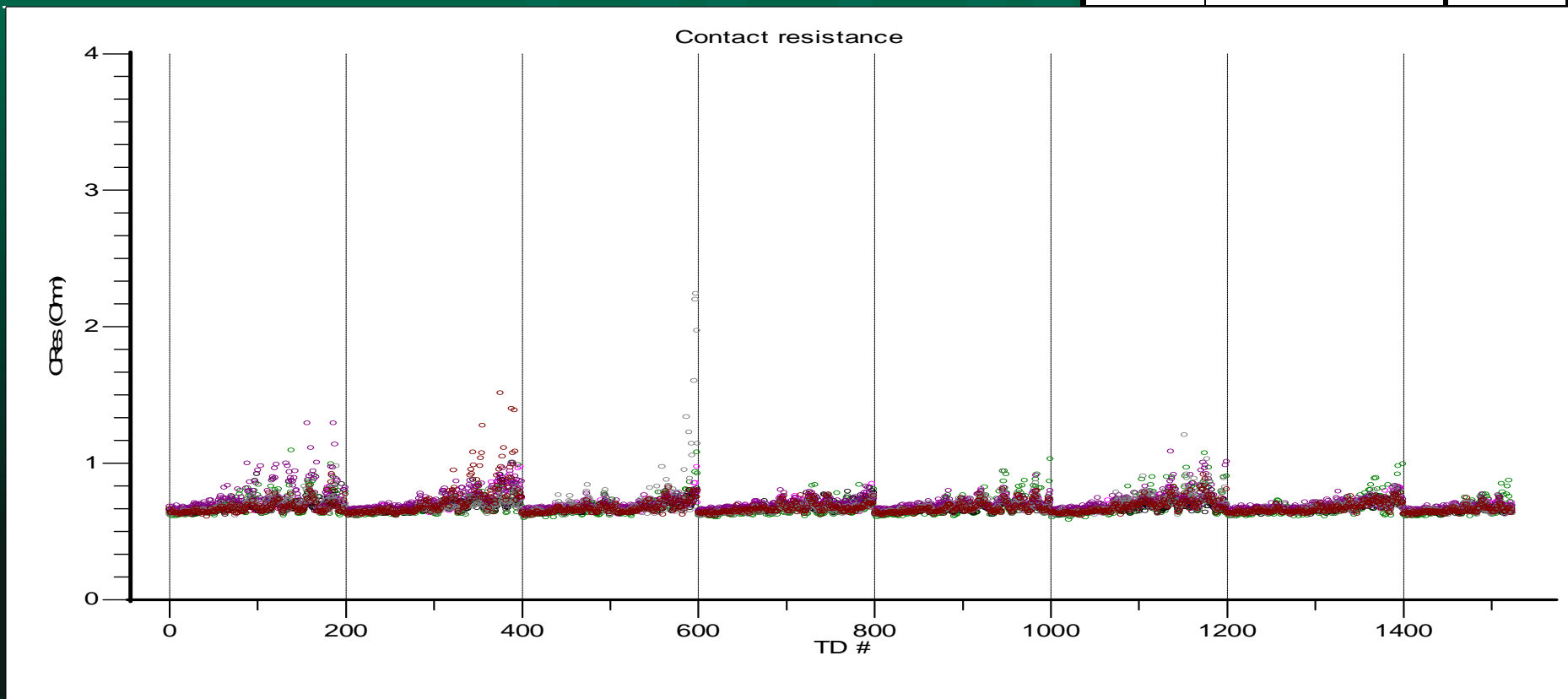


- Low-force probes provide acceptable probe mark at various OD conditions
- 50-60 μ m overdrive is sufficient for CuP production set-up

Contact Resistance (Cres) Stability

- **Demonstrated stable contact resistance of $< 2 \Omega$**
 - No bin failures because of good Cres
 - Cres criteria for bin fails $> 10 \Omega$
- **On-line cleaning every 200TDs with 3um lapping film**

| Cleaning parameters | |
|---------------------|------------------|
| Test OD | |
| | 50 μm |
| Cleaning | OD |
| | 50 μm |
| | Octagon movement |
| | 50 μm |
| # of octagons | |
| 5 | |
| Interval | |
| 200 TDs | |

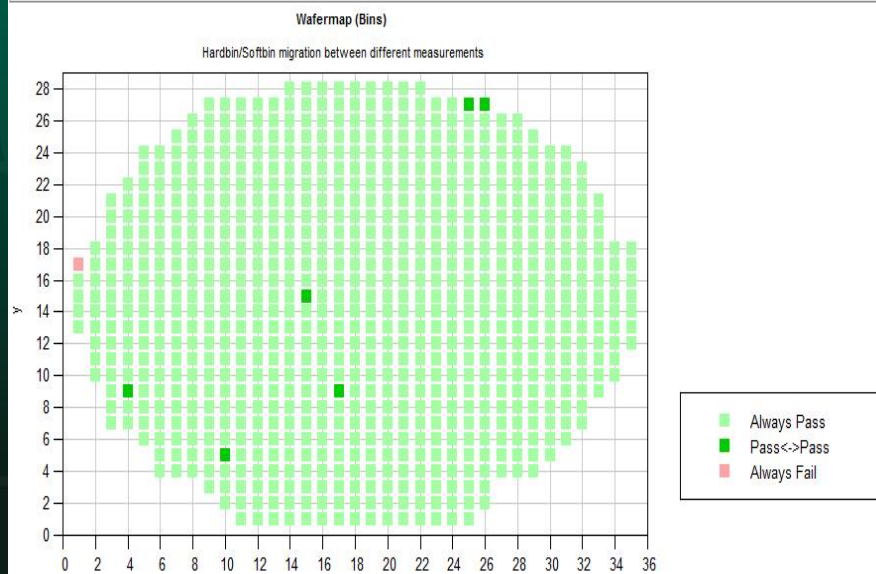


Test Reproducibility: Acceptable Result of >99%

- Same wafer was measured two times to calculate test reproducibility
- Test results from 80 test structures on test chips are used for binning
 - Leakage and resistance measurement with current forcing
 - 10 Ω spec range in most restrictive test structures
- Bin-flips occurred on soft bins
 - 5 bin flips on tests with spec range k Ω
 - 1 bin flip on test with spec range 10 Ω
 - → one flip possibly due to probecard condition
- Acceptable reproducibility of over 99%

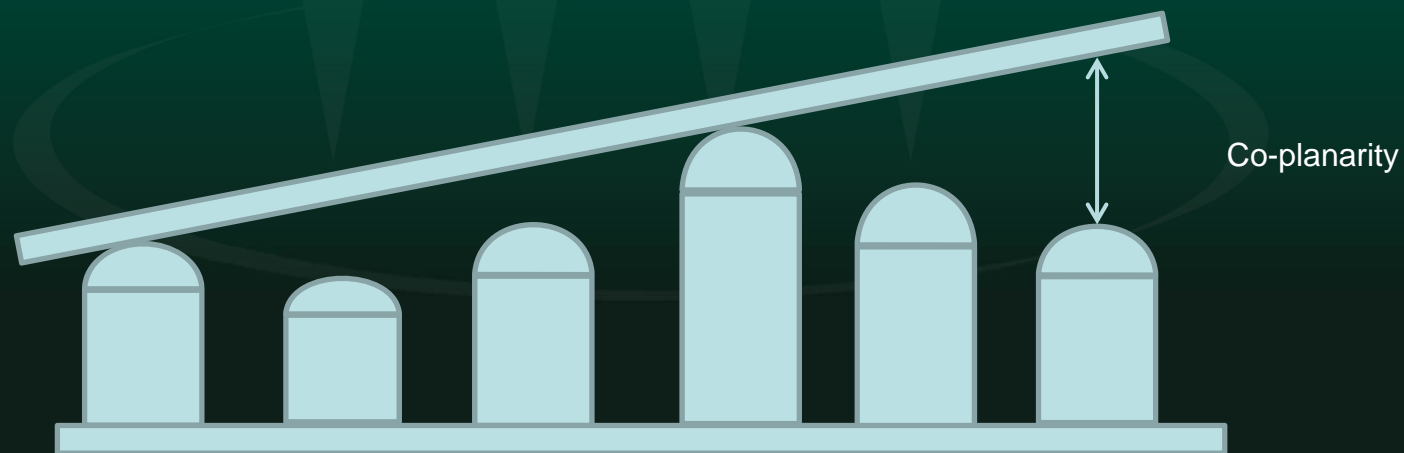
Retest-Quality: 99.2 %

| # systems | % | Category |
|-----------|------|---------------------------------|
| 767 | 99.1 | Always same PASS |
| 1 | 0.1 | Always same FAIL |
| 0 | 0.0 | Change PASS <=> FAIL |
| 0 | 0.0 | Changing FAIL bins |
| 6 | 0.8 | Changing PASS bins |
| 0 | 0.0 | No Hardbin-Information provided |



Co-planarity: Cu Pillars Requirement

- Co-planarity is an established outgoing quality check criteria from bumping houses to ensure packaging reliability
- It is defined as maximum distance from a bump/pillar to the seating plane
- Maximum spec is typically 20 μm or better
- Packaging fails (non-wet) seen for $> 25 \mu\text{m}$ on SnAg bumps

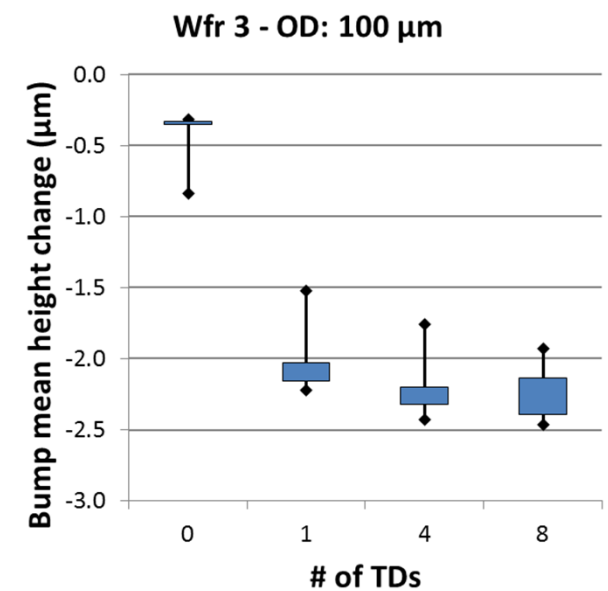
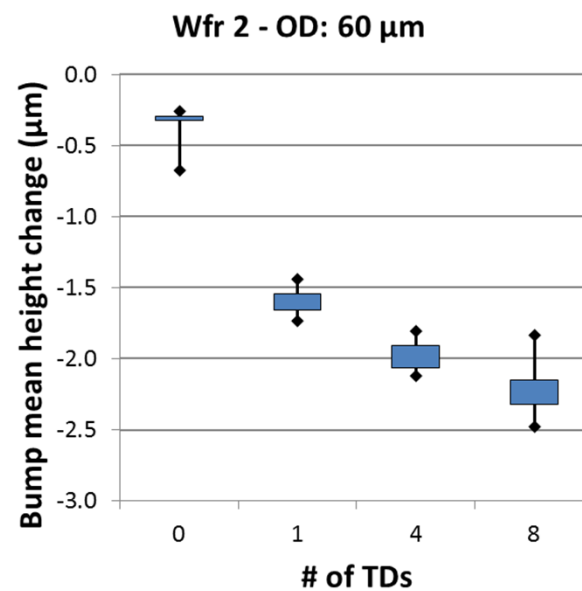
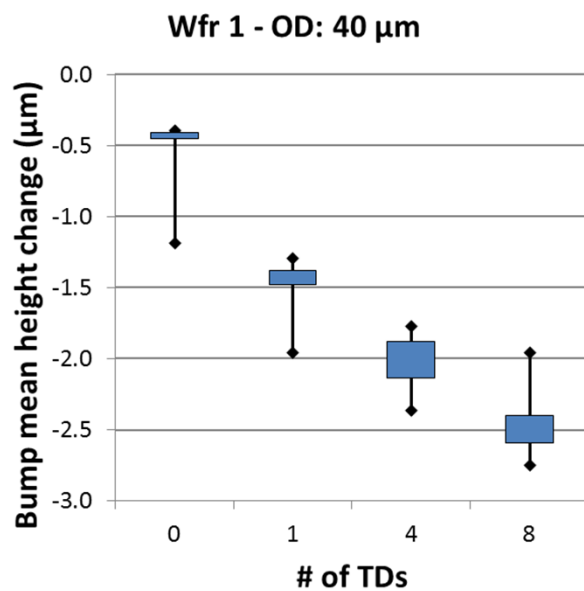


Co-planarity: Probe Conditions to Validate Co-planarity Before & After Probing

- Coplanarity was measured on three wafers before and after probing
- Automated 100% 3D inspection (laser triangulation)
- Probing conditions:
 - Wafer 1: OD 40 μ m, TDs: 0, 1, 4, 8
 - Wafer 2: OD 60 μ m, TDs: 0, 1, 4, 8
 - Wafer 3: OD 100 μ m, TDs: 0, 1, 4, 8

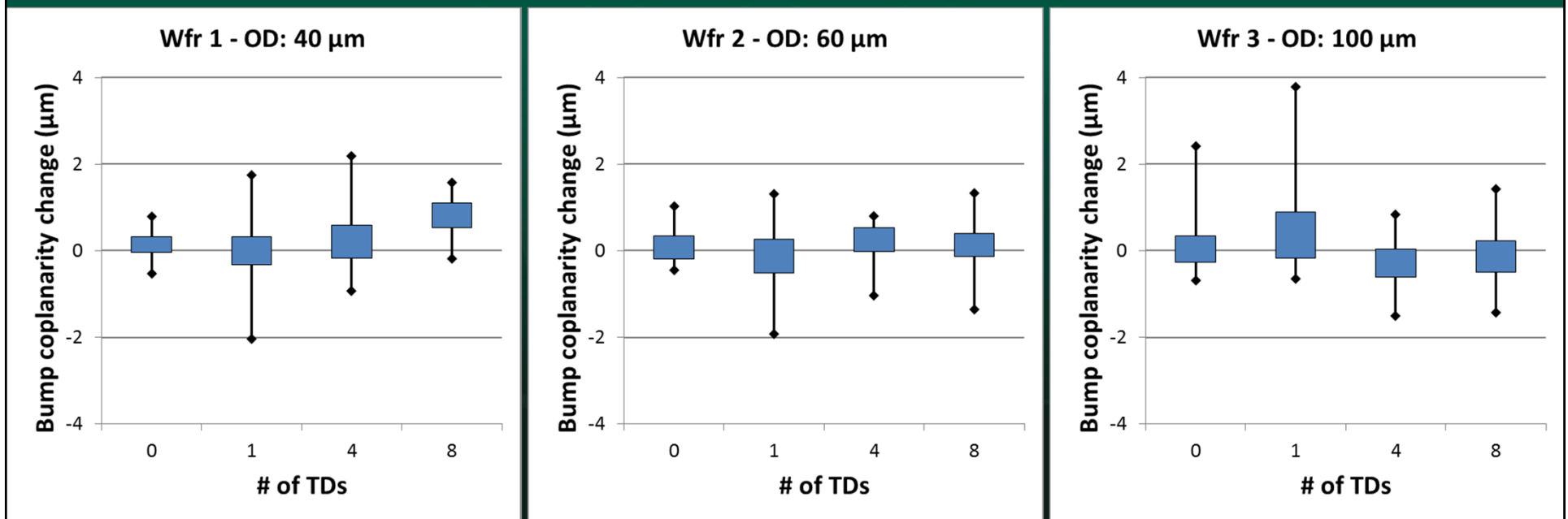
Coplanarity: Bump Height Reduces With An Increase in Probing Touchdowns

- Bump height reduces $< 3 \mu\text{m}$ ($< 10\%$ SnAg cap height) with 8 probing touch downs
- No noticeable SnAg material reduction



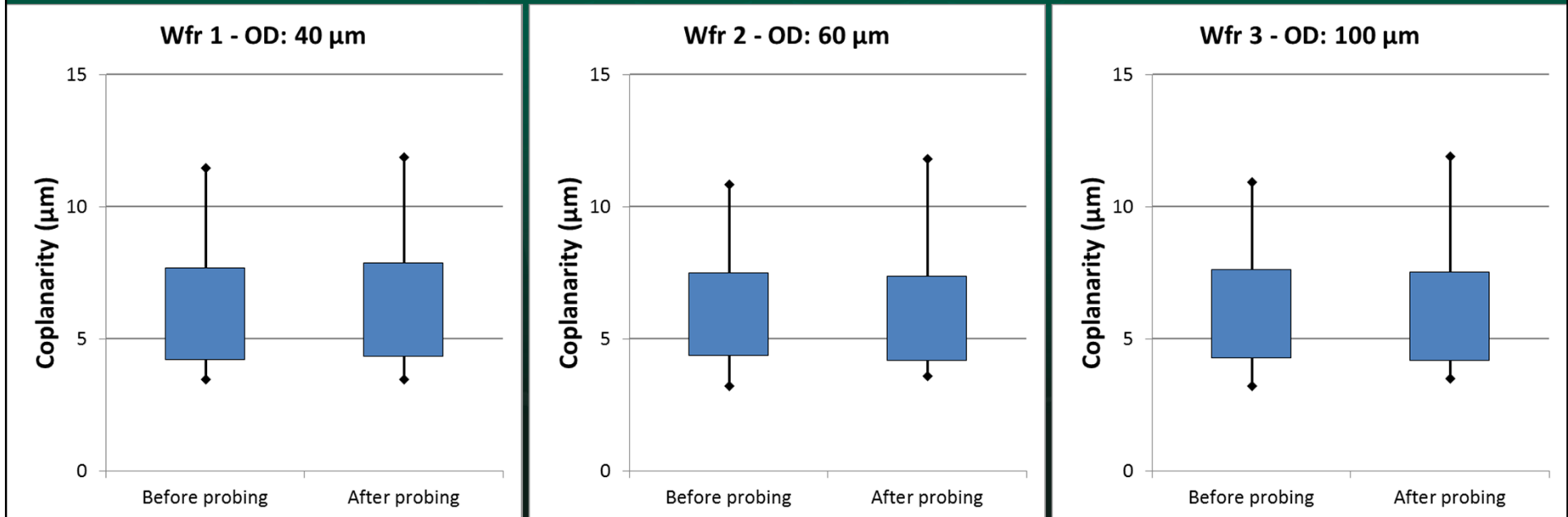
Co-planarity: No Substantial Co-planarity Change Post Probing

- Co-planarity change before and after probing is minimal



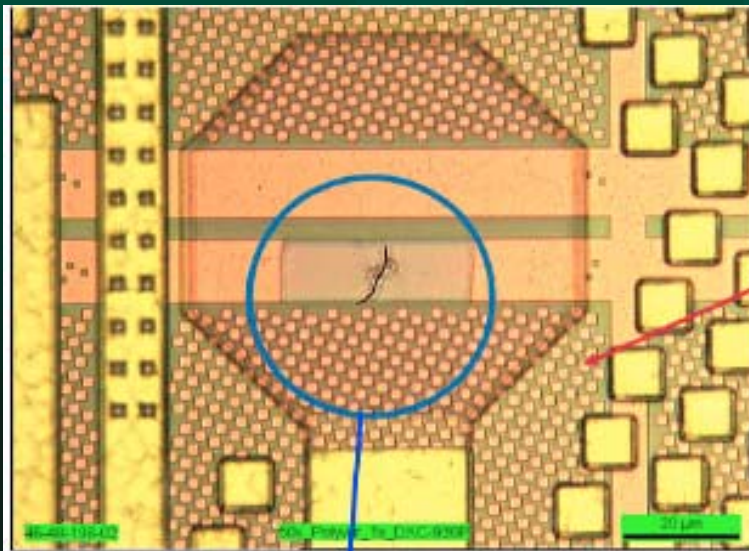
Coplanarity: Overall Co-planarity Meet Bump House Reliability Check

- Probing process, with up to 8 touch downs, did not change pillar co-planarity significantly
- Wafers showed comparable final co-planarity range of <10 μm as the initial pillar condition before probing



Future work

- Investigation on under-pads crack generation after worst case probing, PoAA reliability characterization
- Monitoring in production environment to ensure lifetime requirement (>1M TDs)



Previous example of an under-pad crack observed on 65nm Mobile SoC

Conclusion

- **Implementation of Cu pillar with SnAg caps allows vertical probe card as used to probe on SnAg bumps**
 - MicroProbe low-force Apollo™ vertical product is a qualified solution
 - 2.5 mil probe geometry is a preferred configuration for 120um pitch
- **Low-force Apollo™ product has demonstrated robust performance on fine-pitch grid-array Cu pillar for:**
 - Contact stability
 - Test reproducibility
 - Bump damage
- **Future work**
 - Confirm PoAA reliability
 - Optimize production probecard lifetime