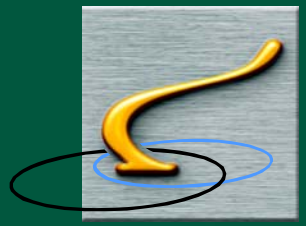
IEEE SW Test Workshop

Semiconductor Wafer Test Workshop



FormFactor®

40k Probes on 300mm

Another Step Towards 1 Touchdown DRAM SORT

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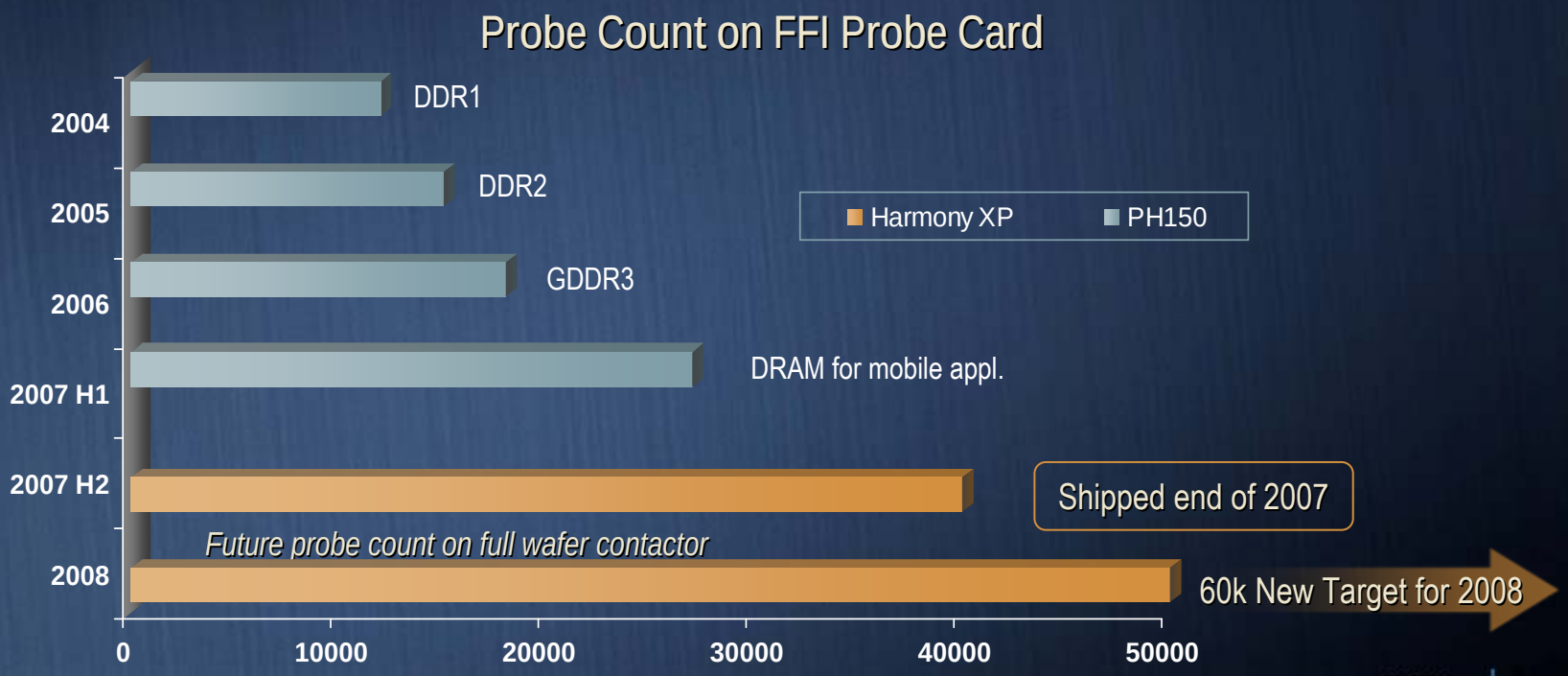
San Diego, CA USA | June 10, 2008

Outline

- Recap from last year: 26k probes – a new dimension in probe count
- What's new?
  - Roadmap for probe count
  - DRAM trends
- Roadmap to 1 touchdown DRAM SORT
- 40k probes on 300mm area – results and field data

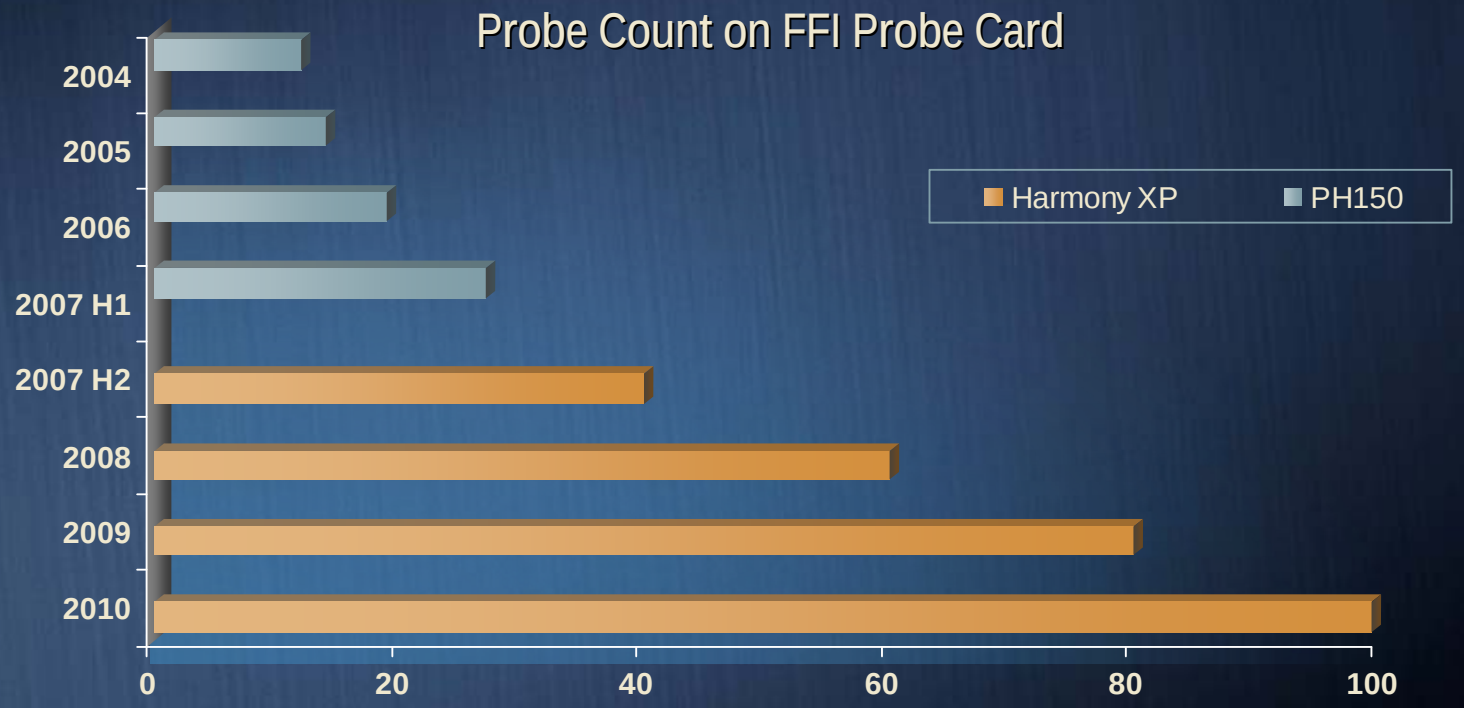
Industry Probe Count Trend (as shown 2007)

- Total probe count has increased significantly in recent years
- This increase was not driven by increasing parallelism until 2006
- However parallelism is increasing to 384 DUT and higher
  - This will act as a multiplier on the total probe count leading to 40 - 50k probes



Industry Probe Count Trend 2008

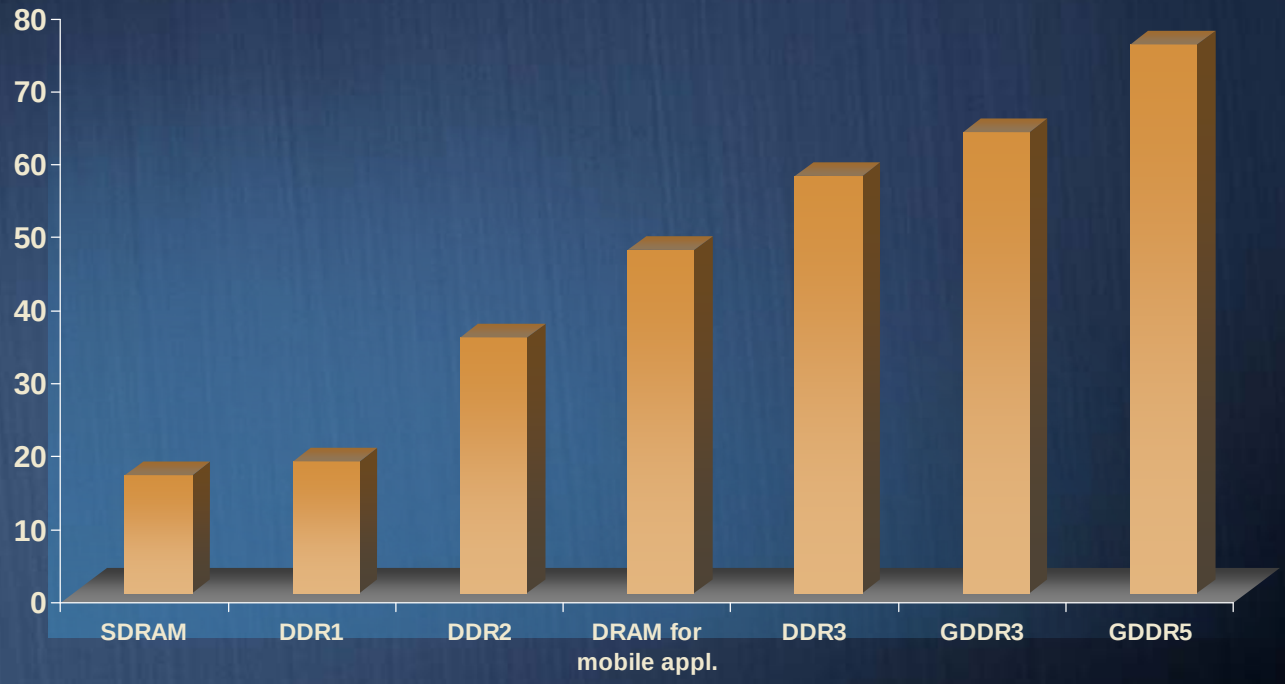
- Increase in parallel test will boost total probe count
  - Parallel test has already exceeded 384DUT for SORT
- Signal count per DUT will decrease but number of power and ground probes will increase further



Data based on FFI's entire customer base

Industry Probe Count Trend (2008 – cont.)

- Increase in number of probes for Power and Ground
  - ~60% of all probes are power and ground today
  - New device architectures
  - Lower supply voltages and higher frequency
  - Impedance of the power delivery system (see last year's presentation)



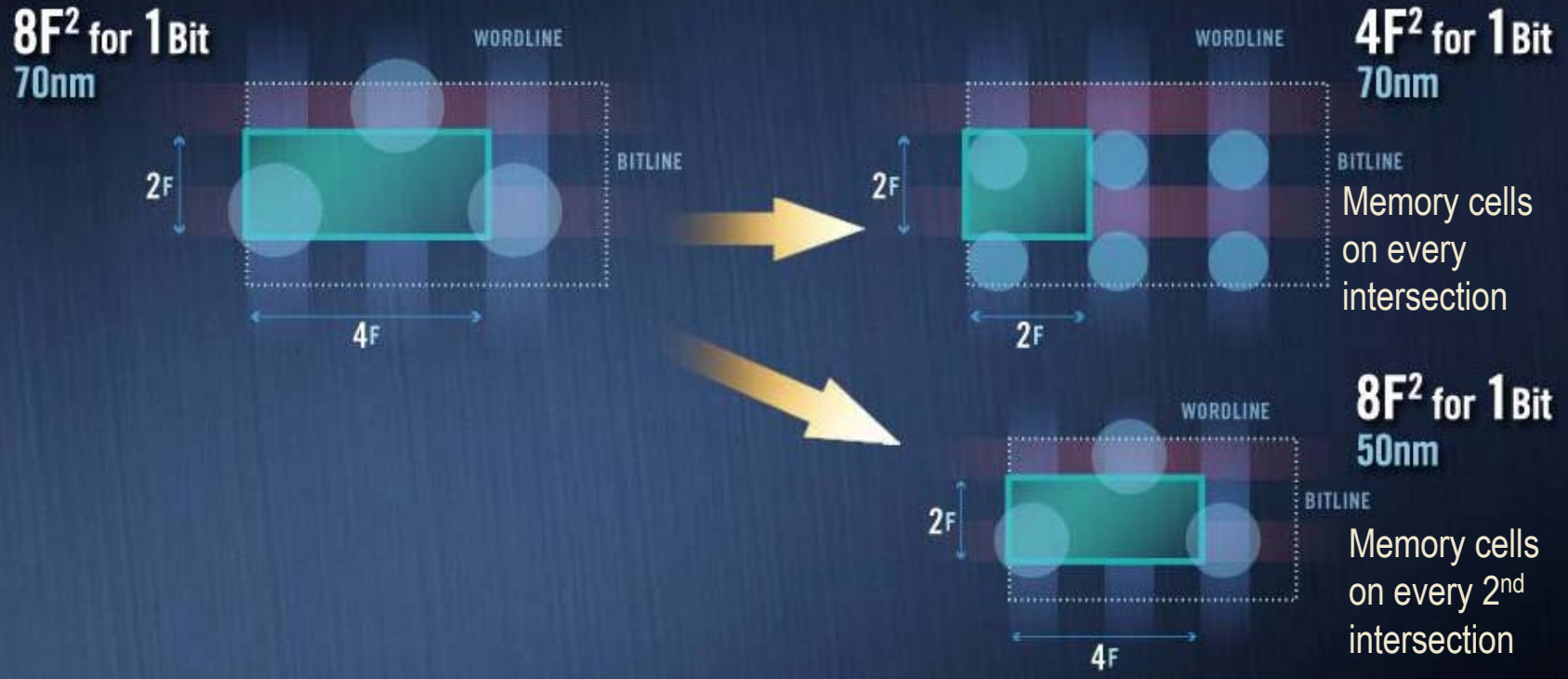
Data based on FFI's entire customer base

What's New? – Industry Drivers

- DRAM price has decreased dramatically in 2008
- Production cost is the number one issue
  - Shrink faster to get more die per wafer
    - New technology nodes
    - New design rules $8F^2$ – $6\ F^2$ – $4\ F^2$
    - Die size is getting smaller
    - Pad size and pitch need to get smaller
      - Accelerated by trend to more efficient LOC pad layout
  - Test cost is under pressure as well
    - Increase parallel test
    - Make more use out of existing test equipment
    - Test time reduction efforts and uptime improvement projects

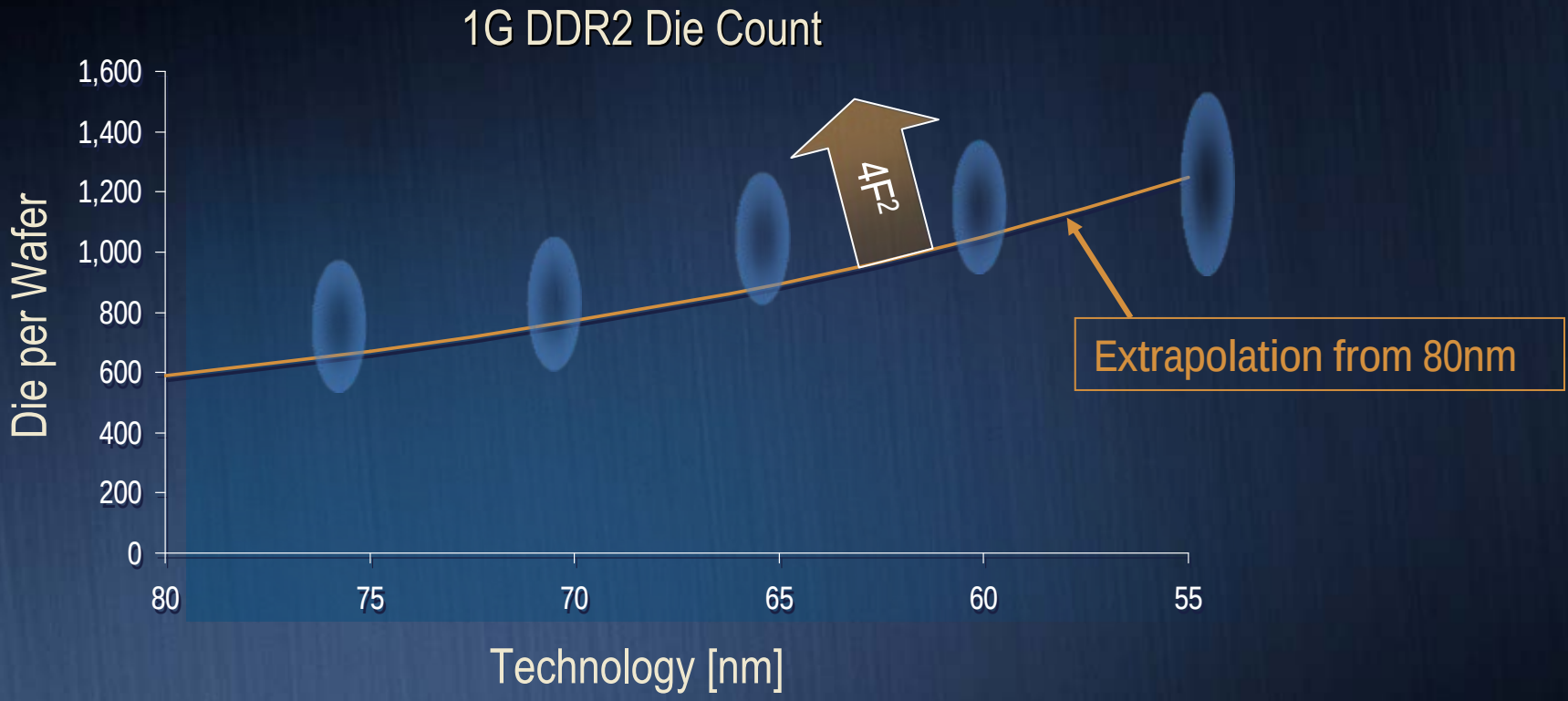
New Design Rules for DRAM – $4F^2$

- What is 8F2, 6F2 and 4F2 ?
  - It describes the area needed for one Memory cell



- A change from 8F2 to 4F2 gets the same die size reduction as a shrink from 70nm to 50nm

Increasing Die per Wafer

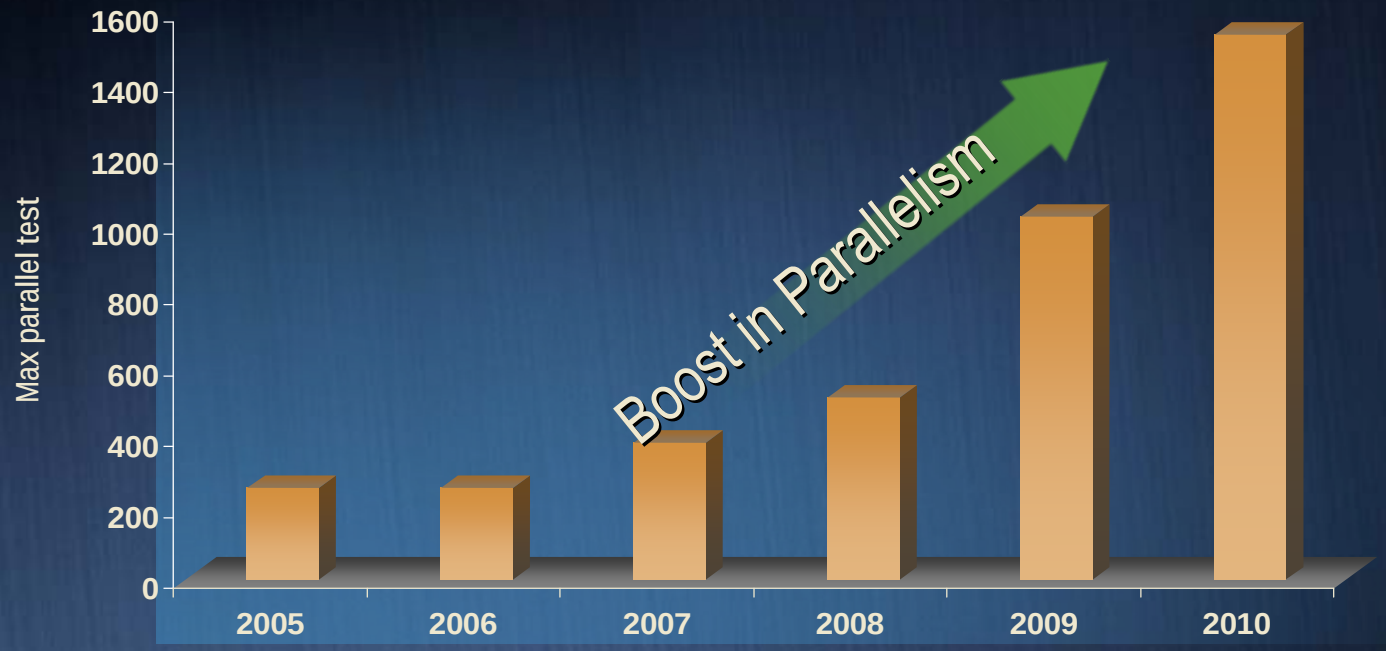


- Number of DRAM die per wafer in HVM typically was 700 -1500
  - Once this number was reached Memory density doubled, e.g. 512M to 1G
- This will increase to 1000 – 1800 with new design rules
- Touchdown count would increase in case parallel test stays flat

New design rules for DRAM: DLOC to LOC

- More efficient pad layouts enabled by smaller pitch and pad size
- Increasing pad count has forced many DRAM design to DLOC
- Smaller pad pitch and pad size allow LOC design
  - Die size reduction between 80 and 100µm
  - Up to 2% more die per wafer
  - Biggest pad size reduction is needed in non scrub direction (X-direction)

Increasing Parallel Test – Road to 1 TD



- New testers with higher channel counts will be introduced in the next 2 years
- New test strategies and advanced TRE are pushing parallel test further
- Still 1 TD will be hard to achieve due to the increasing die count and more complex probe card design (routing density, noise sensitivity …)

Probe Card with 40k Probes

Harmony XP Probe Card with 40k Probes

- Probe count = 40k probes
  - Built out of 4 probe heads with 10k probes each
  - FFI has built more than 26k probes on PH150XP
    - Even 100k are possible on Harmony XP with the existing architecture
- Probing area: 300mm diameter
- Used for WLBI of DRAM chips: 1 TD
  - Ultra parallel test can be achieved more easily due to higher level DFT
  - Less probes per DUT but much high parallelism
  - Used at higher temperature than DRAM SORT
- Different designs were built with probe count in the 40k range for different customers in 2007 and 2008

System Deflection

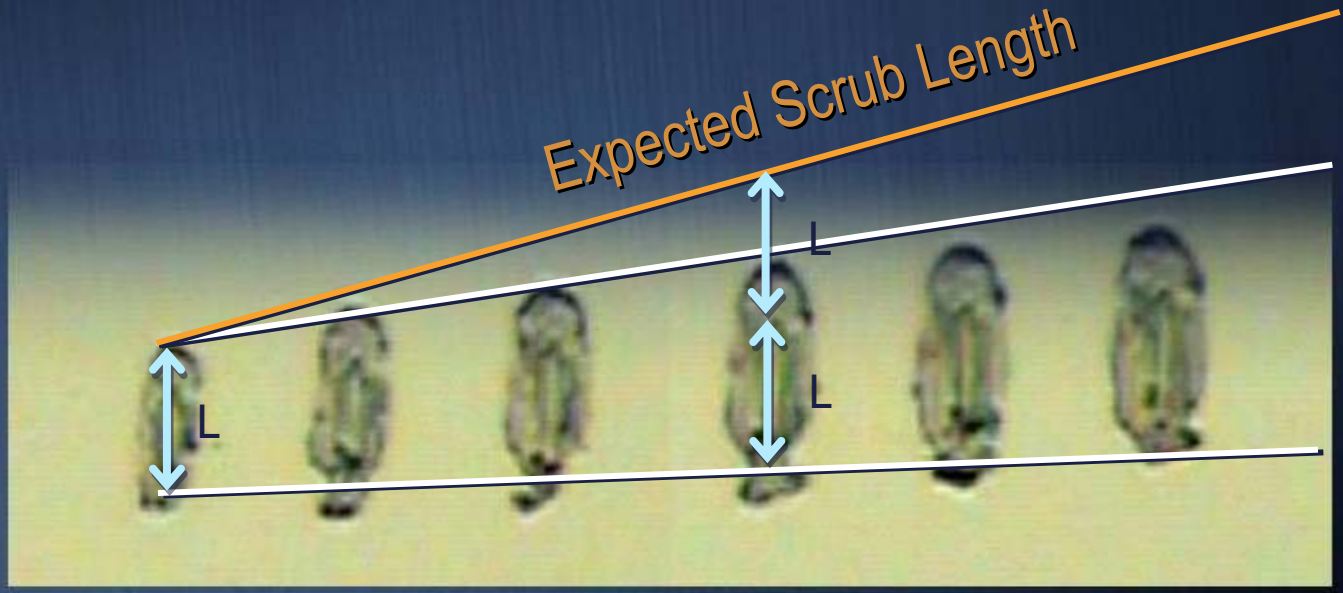
- System deflection is the biggest concern from the user
- High probe count probe cards create a significant force which leads to deflection in the whole test cell
  - Deflection of the probe card itself
  - Deflection of the chuck
  - Deflection of the head plate
  - Coupling between wafer motherboard and prober head plate
- System deflection is define as AOT/POT ratio
  - Actual Over Travel / Programmed Over Travel
- How much of the programmed over travel is really achieved on each probe?

System Deflection

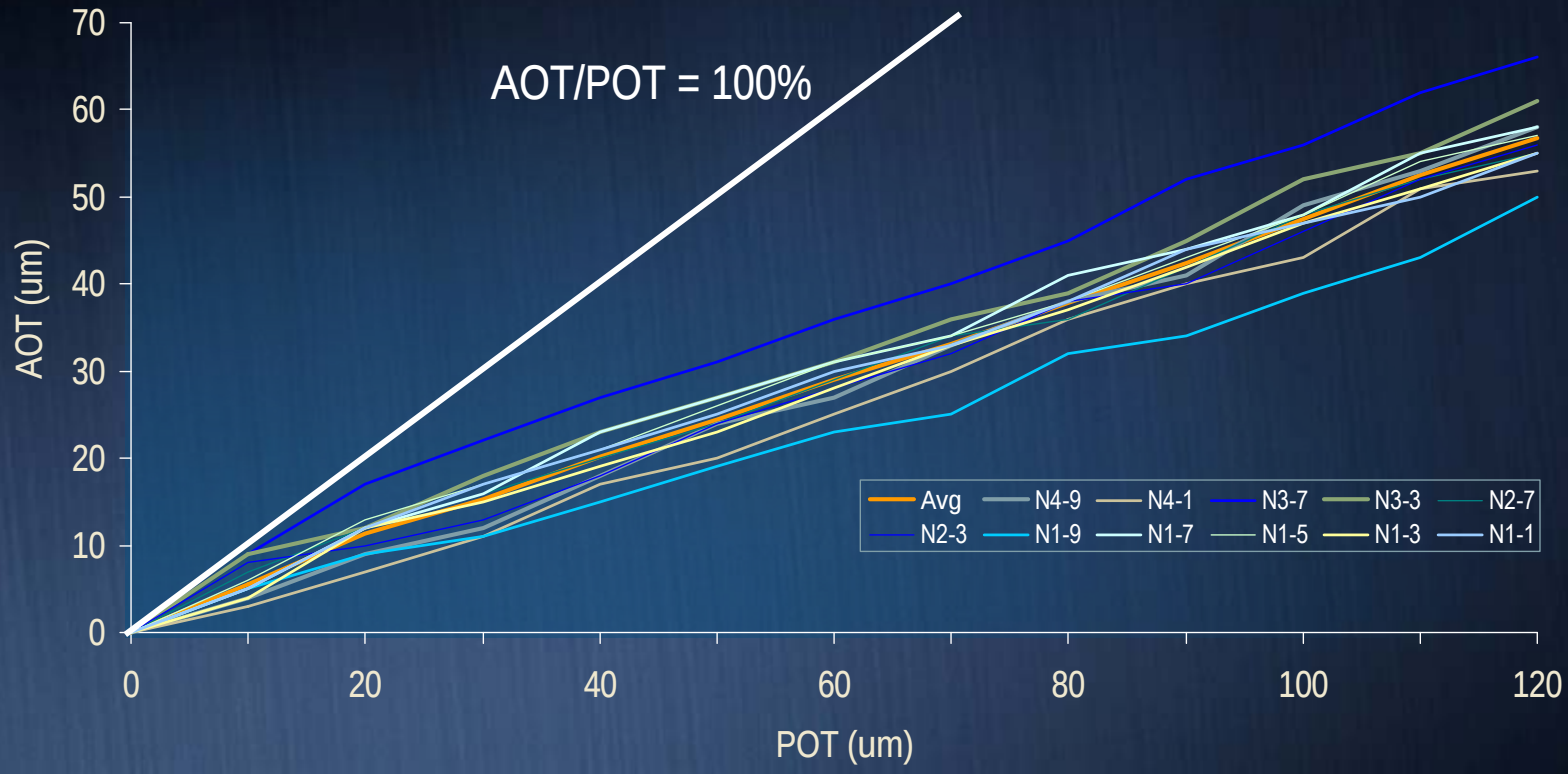
- Different measurement techniques are used to characterize system deflection e.g.:
  - Laser interferometer
  - Scrub mark analysis
  - Micro sensor
- Many different prober / tester / docking combinations were investigated at various customer installations and at FFI application lab
- Depending on the probe count and the test cell a AOT/POT ratio between 25% and 80% was found for probe cards between 20k and 40k probes
- For 40k probe count the best system showed AOT/POT of ~50%

System Deflection – Scrub Mark Analysis

- Scrub length is analyzed as a function of programmed over travel
- Knowing the probe scrub ratio the actual over travel can be determined



System Deflection – Typical Results



- AOT/POT measurement showing a 50% AOT/POT using a 40k pin probe card

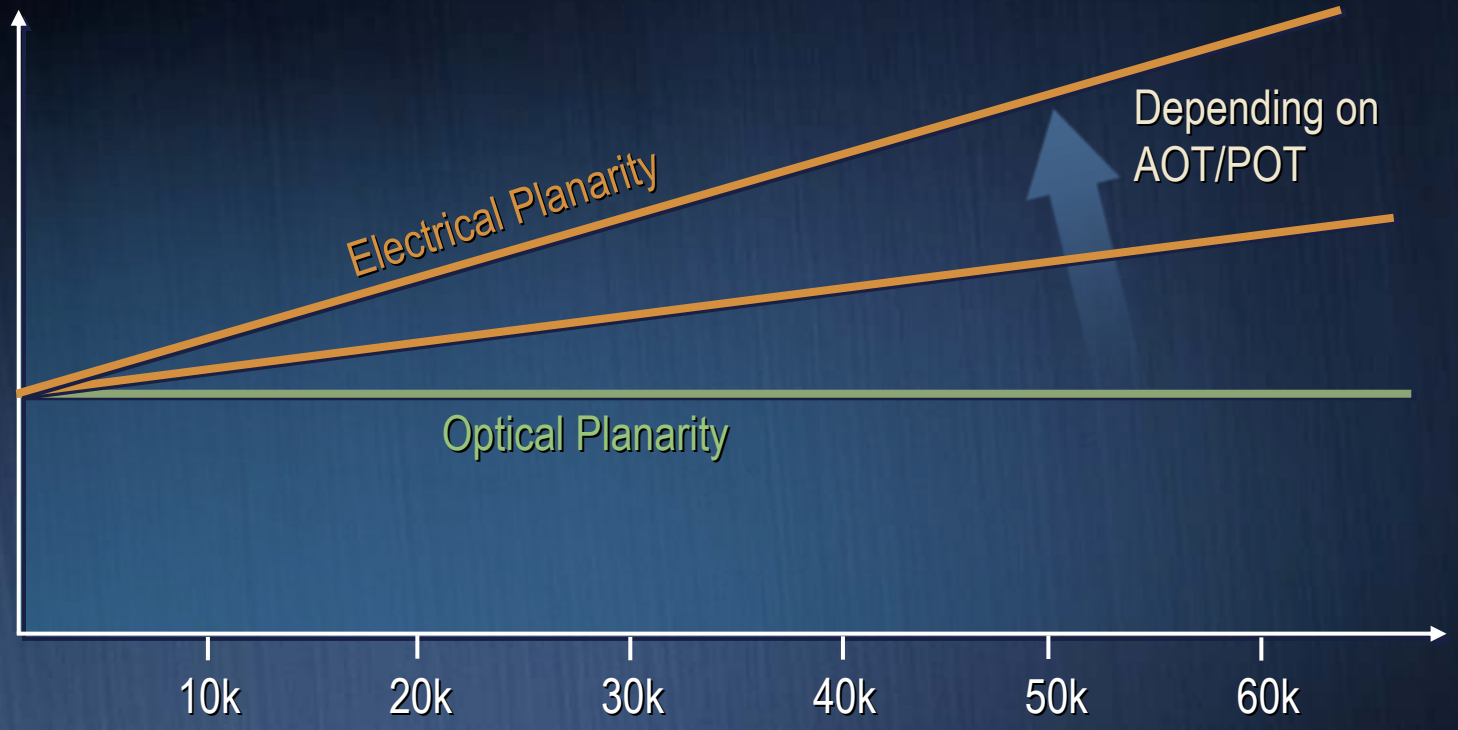
Planarity and System Deflection

- Electrical Planarity is used as a measure for characterizing probe card performance
- With smaller probe count and less system deflection optical and electrical planarity were very close
- This has changed with high probe count probe card

$$\text{Electrical Planarity} \sim \text{Optical Planarity} \,/\, (\text{AOT/POT})$$

- Planarity specifications need to be changed

Planarity and System Deflection



- Also the programmed over travel needed for stable Cres needs to be adjusted because of the deflection
- Learning process is required

Probe Card with 40k Probes - Results

- Used in volume production
  - Stable and consistent Yield results
- Other designs with similar probe count are currently built
- First experiments with 60k probe cards will start soon

Summary

- Probe count will continue to increase in the next few years
  - New chip architectures
  - Increase in parallel test
    - New tester
    - New test strategies
- Overall system deflection will require a different view on
  - Electrical planarity
  - Programmed Over Travel needed for good test results
- Strong cooperation between tester, prober, prober card companies is required to address the system aspect of the problem

Acknowledgements

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