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A Flexible Vertical MEMs Probe Card Technology for Pre-Bump and eWLP Applications

MICROPROBE
Relentlessly Delivering Results

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Vertical MEMS for Pre-Bump Probe

- **Introduction: eWLP and Pre-Bump Probing Requirements**
- **Experiment Objectives & Details**
  - Accurate Probing on Small Pads at Fine Pitch
  - Low Scrub Depth on Pre-Bump Pads
  - Wafers Probed & Measurements Taken
- **Observed Probe Results & Conclusions**
  - Accuracy & Repeatability Across Wafer
  - Measured Scrub Depth Results
  - Reliable Enabling of Pre-Bump Probing for Improved eWLP Yields
- **Follow-On Work**
  - Production Characterization in Large Volume
- **Summary**

MicroProbe: A Leading Supplier of Logic/RF/SoC Probe Card Solutions

Innovation and Growth

- **Technology Leadership**
  - >1000 MEMS probe cards delivered
- **Market Share Growth**
  - #1 supplier of Advanced SoC Probe Cards
- **Customer Collaboration**
  - 35-year history of delivering results

Breadth and Stability

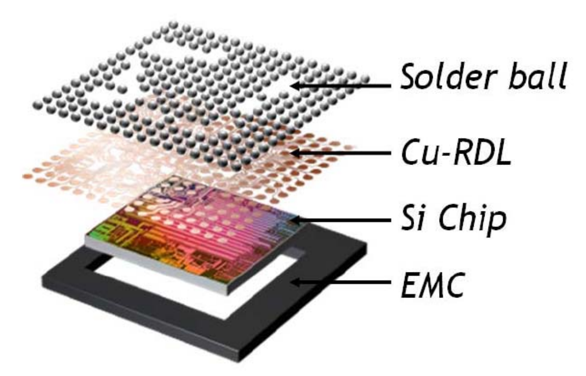
- **Broad Product Portfolio**
  - Cantilever, Vertical, and MEMS
- **Global Presence**
  - Major facilities in China, Taiwan, US
- **Strong Institutional Investors**
  - Flywheel Ventures, Gemini Investors, Intel Capital

eWLP Resurrects Pre-Bump Array Probing

- While pre-bump probing has been largely eliminated from mature BGA Flip-Chip packaging flows, the workflow and cost considerations of eWLP are re-introducing need for effective pre-bump probing on arrays of aluminum pads.
- Today's designs challenge probing on multiple fronts:
  - Full-grid array layout at ~100um pitches → **Vertical Architecture**
  - Small pads and pad openings → **Small Scrub**
  - Low-k dielectrics and under-pad circuitry → **Low Force**
- Experimental work demonstrates that MicroProbe's MEMS Vertical probe solution addresses today's pre-bump probe requirements, enabling cost-effective implementation of newly developed eWLP-based packaging flows.

What is eWLP?

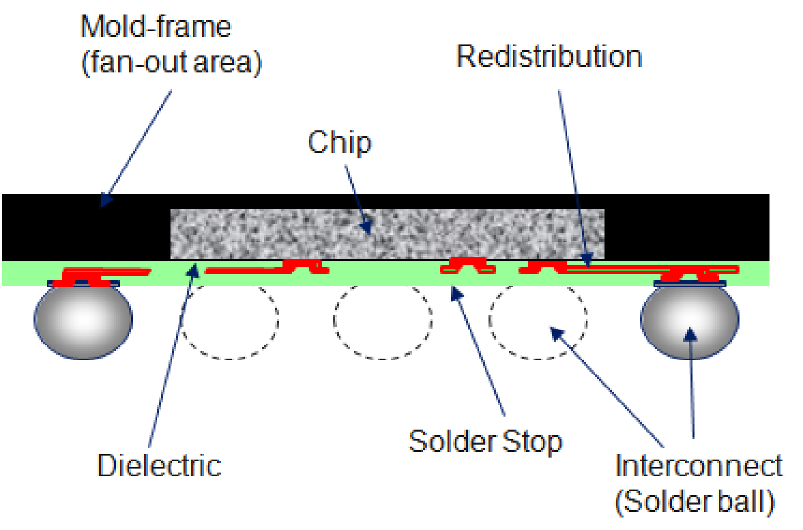
- eWLP = “Embedded Wafer Level Packaging”
- eWLP is an evolution of BGA-type packaging that uses molded carriers and fan-out RDLs. The original die are singulated, embedded into molded carriers, and then reconstituted onto artificial wafers. Wafer-level processes then add redistribution layers (RDLs) and solder balls
- This approach enables both a higher level of interconnects per die area (due to the fan-out RDL) and enables greatly simplified multi-chip integration.
- Also known as eWLB (Wafer-Level BGA) and FO-WLP (Fan-Our WLP)



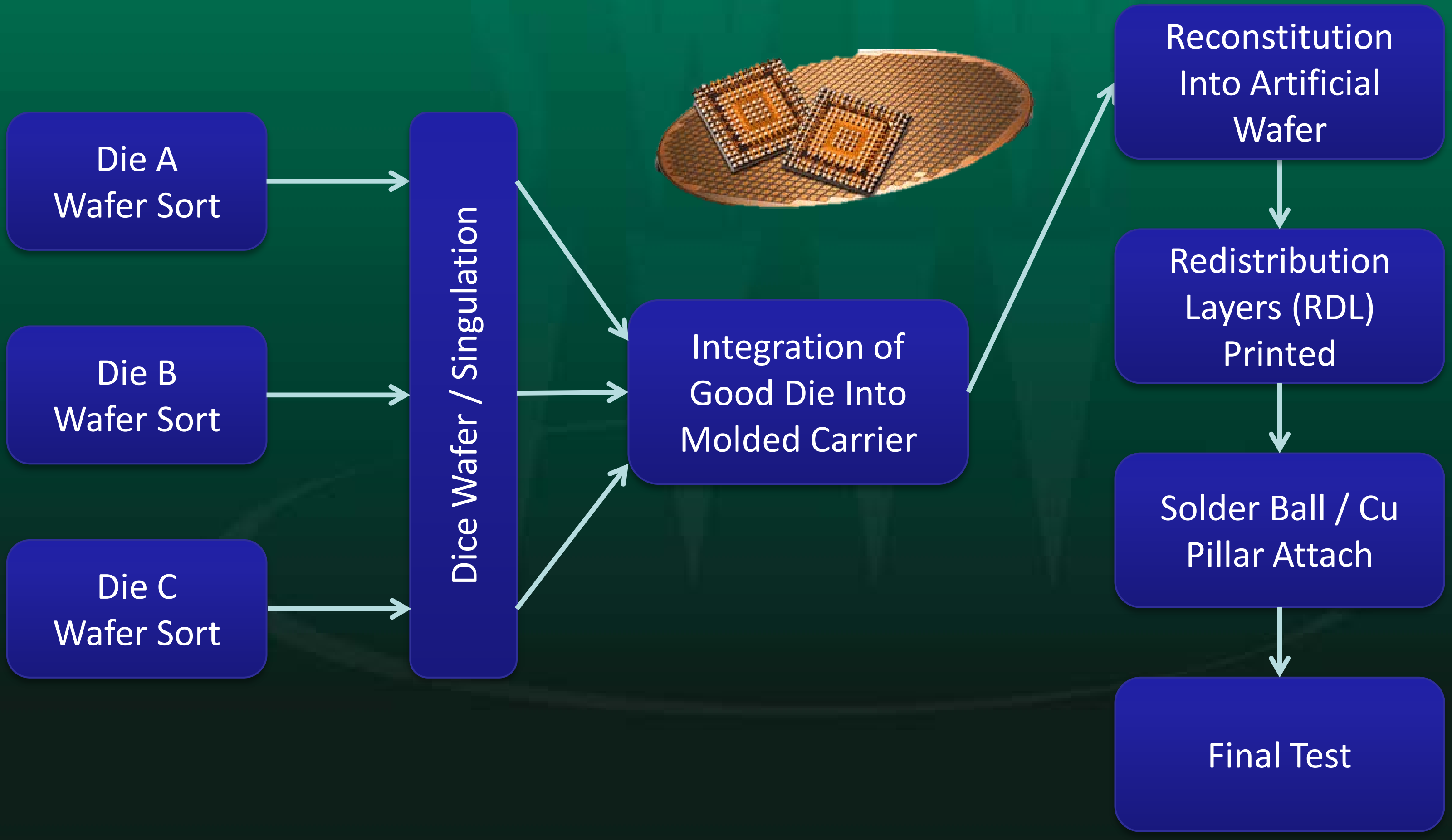
A Simplified eWLP Stack-Up

eWLP and Pre-Bump Probe

- Packaging bad die into molded carriers, and subsequently attaching them to reconstituted wafers, causes very expensive yield loss for the final eWLP wafer.
- For multi-die eWLP packages, the cost impact is even worse – the problem is directly analogous to test escapes finding their way into a multi-chip module.
- Because of these considerations, effective test of the target die prior to singulation is imperative to ensure good yield at final test.



Example eWLP Test Flow



Die A
Wafer Sort

Die B
Wafer Sort

Die C
Wafer Sort

Dice Wafer / Singulation

Integration of Good Die Into Molded Carrier

Reconstitution Into Artificial Wafer

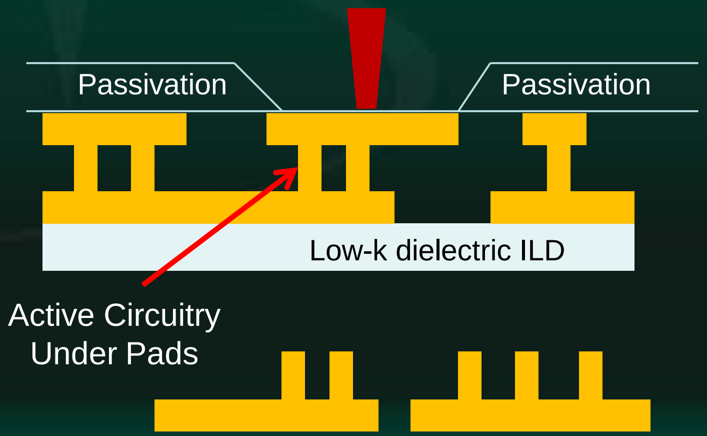
Redistribution Layers (RDL) Printed

Solder Ball / Cu Pillar Attach

Final Test

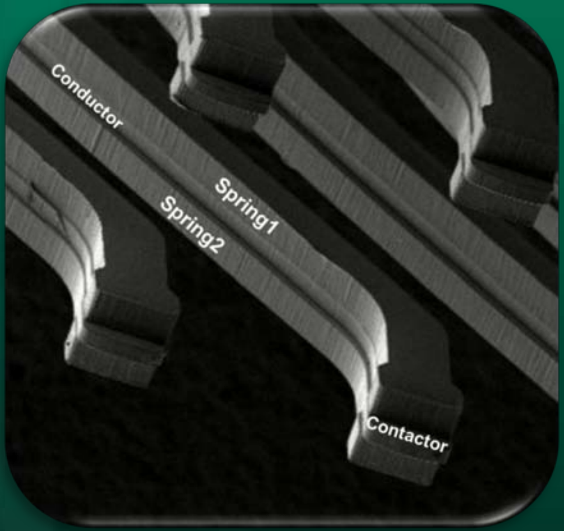
Pre-Bump Probe Challenges

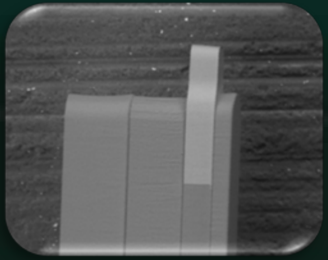
- Fine Pitch in Full Grid Arrays
  - RDL fan-out permits increasingly fine pitch across high pincount arrays. Today's arrays are 130um – 180um. Next generation arrays will be < 100um.
- Small Pads
  - Bond pad openings are getting smaller: 50um octagonal pads are migrating towards 40um
- Low Force
  - CUP and Low-K require very low force contact on the pad material to ensure there is no IC damage



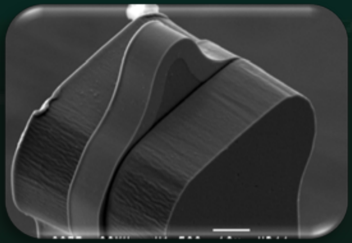
MicroProbe Vertical MEMS "Mx" Probe Architecture

- **Composite MEMS structure allows optimization of mechanical and electrical design**
  - Multiple materials & Layers
  - Photolithographically Defined Shape
- **Resulting material & geometry flexibility provides optimal contact performance and pitch scalability**





Mx-FP Probe
Low-K / CUP

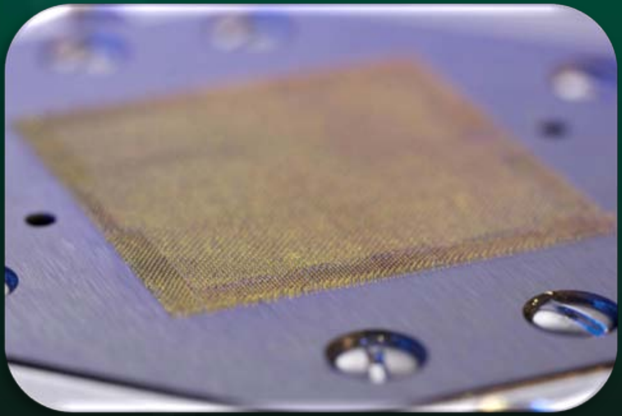


Pointed Probe
Al & Cu Pads

Flat Probe
Cu Pillars, Bumps

Customer Experiments with Mx for Pre-Bump Probing

- Customer A: Focus on low force contact to minimize pressure applied to circuit under pad
- Customer B: Focus on good contact with minimal scrub depth into pad material
- Customer C: Focus on probe tip accuracy for contacting small pads with high precision and repeatability



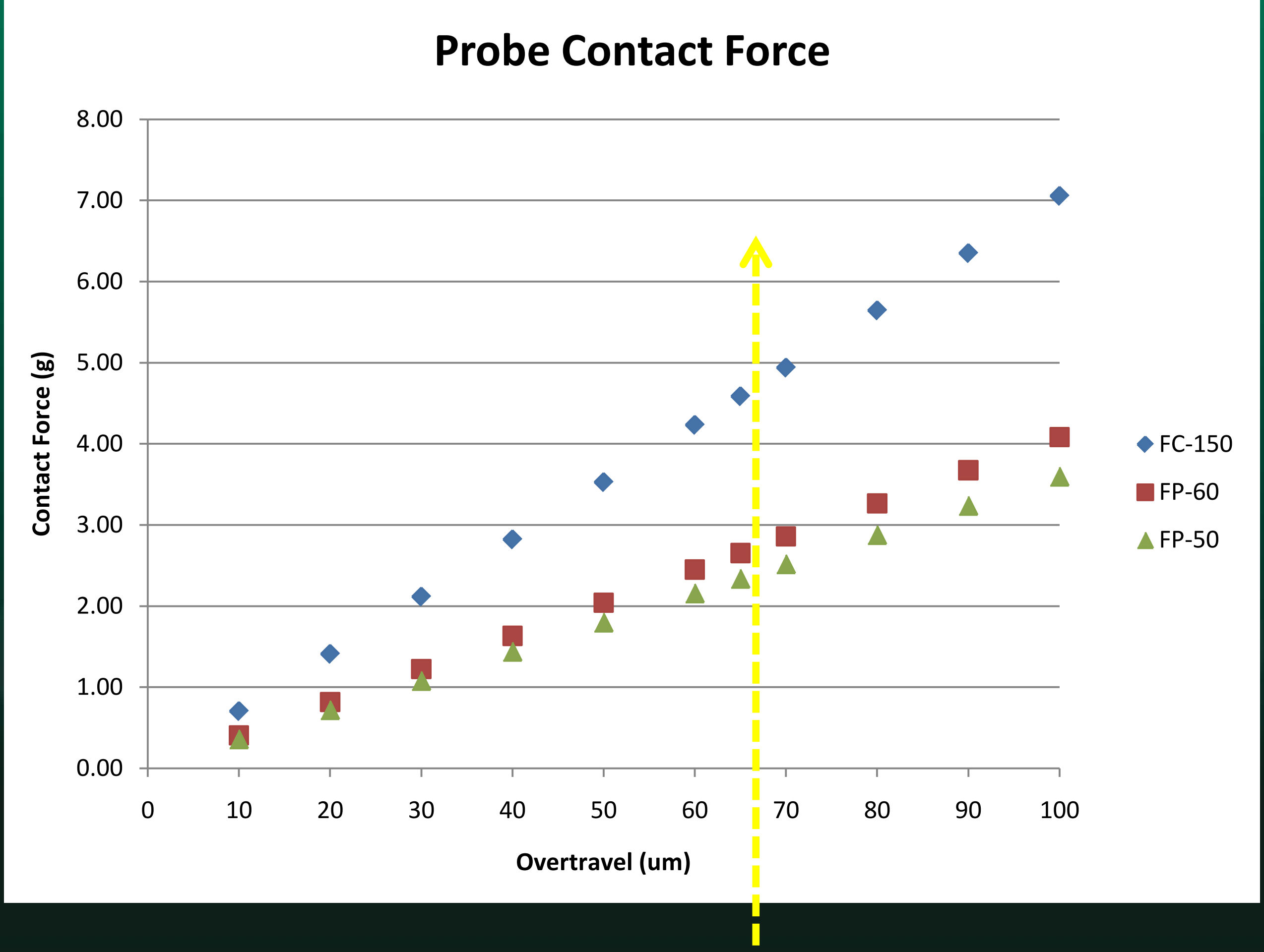
Example Mx Probe Head with > 10K MEMS Probes

Customer A: Low Force Experiment

- Wafer Setup for Experiment
  - 300mm wafer at 40nm process
  - eWLP pre-bump pads probing
  - 60um octagonal pads

- Evaluation Criteria
  - Cres must be within acceptable range for device
  - Probe force over active area and low-k ILD must be minimal
  - Scrub mark must be small and repeatable

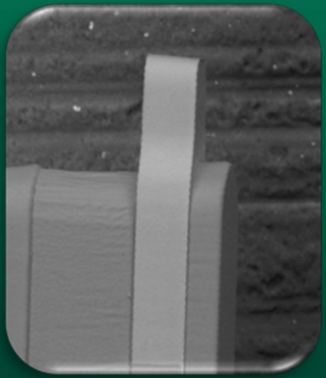
Mx Probe Contact Force at Overtravel



Recommended OT = 65um

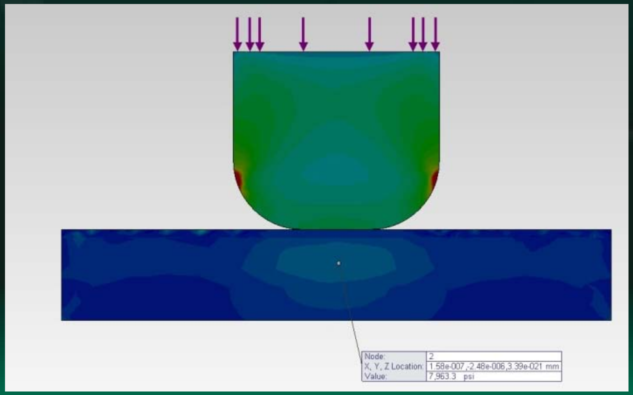
Mx Low-Force Design & Modeling

- MEMS Geometry & Metallurgy
  - Proprietary Mx MEMS process enables multi-layer probe design with lithographically defines shapes
  - Focused on low-force mechanical design while maintaining excellent Cres characteristics



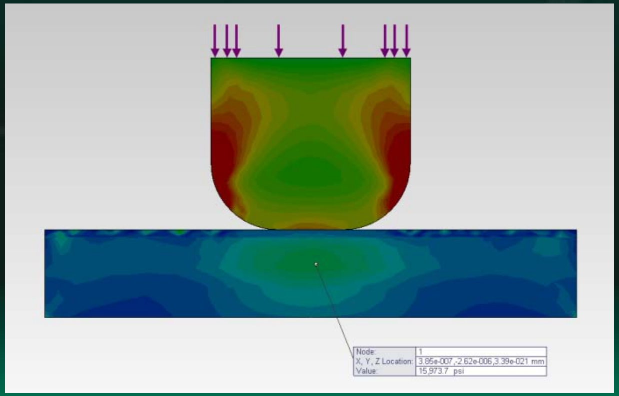
- Design & Modeling
  - Detailed FEA models are developed to predict scrub stress behavior
  - Model predictions are continually refined based on real-world observation

2g contact force



Node: 2
X, Y, Z Location: 1.58e-007 ,-2.48e-006 ,3.39e-021 mm
Value: 7,963.3 psi

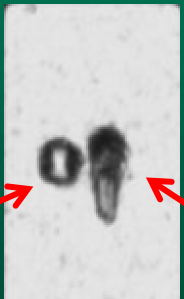
4g contact force



Node: 1
X, Y, Z Location: 3.85e-007 ,-2.62e-006 ,3.39e-021 mm
Value: 15,973.7 psi

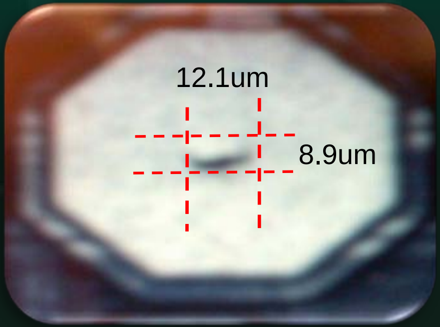
Customer A: Low Force Findings

- Mx scrub mark ranges 8um – 15um
- Maximum scrub depth of 0.55um
  - (After 8 touchdowns)
- No ILD cracking found with 60um over-drive



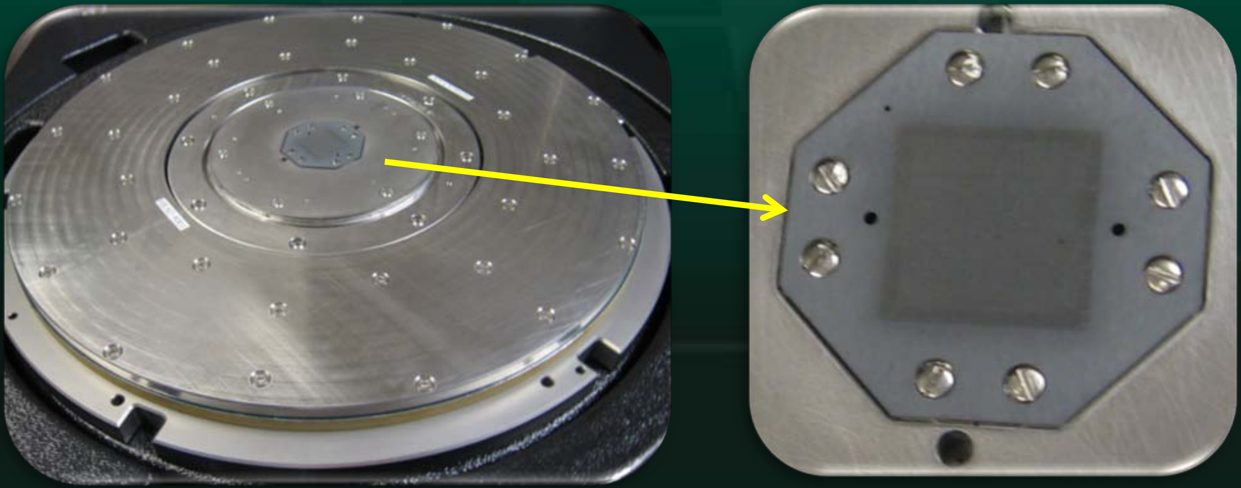
Mx-FP Scrub Length of ~10um

Cantilever Scrub Length of >30um



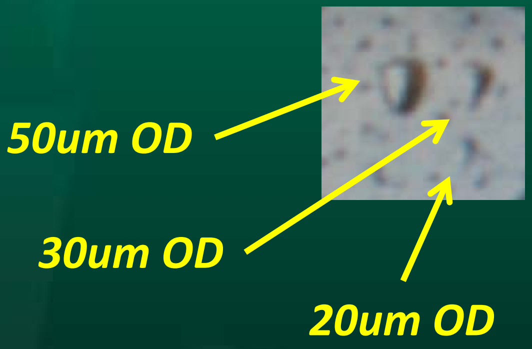
Customer B: Small Pads Experiment

- Test Setup for Experiment
  - ≈180 Die Per Wafer
  - ≈ 7,500 Pads Contacted per Die
  - 55um Pads in 180um Array
  - TEL P12Ln Prober with Test Temperature of 40degC

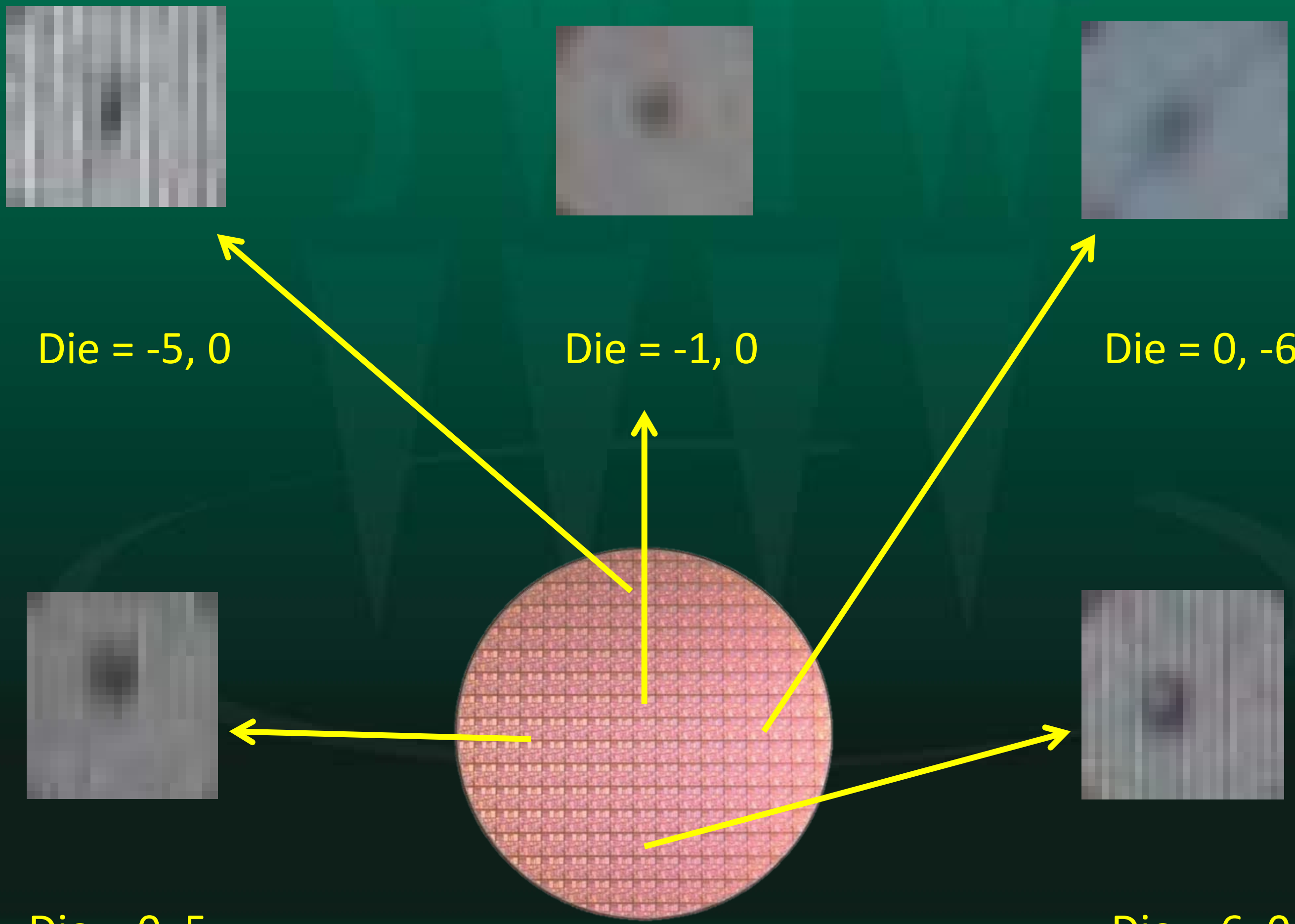


Scrub Mark Size & Accuracy

- Customer Findings on Scrub Mark Placement
  - Typical accuracy to pad center: +/- 9um
  - Worst-case accuracy observed: +20um
  - (Mx Typical Spec = +/-13um)
- Customer Findings on Scrub Mark Size
  - 20um OD → 7um Scrub
  - 30um OD → 10um Scrub
  - 50um OD → 11um Scrub
  - 65um OD → 15um Scrub
  - (Mx Recommended OD = 65um)



Accuracy & Repeatability Across Wafer



Die = -5, 0

Die = -1, 0

Die = 0, -6

Die = 0, 5

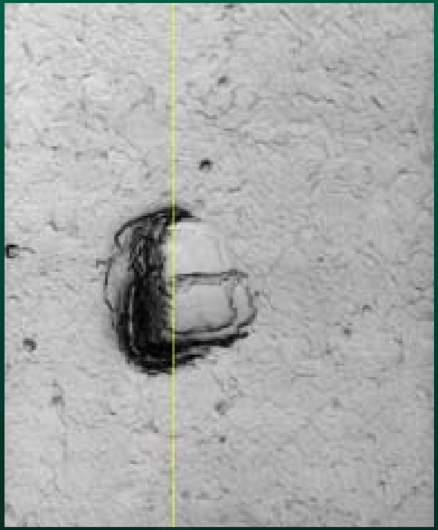
Die = 6, 0

Customer B: Small Pads Findings

- Mx solution delivers highly-accurate and repeatable scrub marks that are suitable for pre-bump probing small pads
  - Overall planarity of a large array was very good (< 24um)
  - Probe mark placement was very accurate, consistently placing the scrub center within +/- 13um. (One outlier was observed.)
  - Placement across 300mm wafer was extremely repeatable
  - Tip recognition, cleaning requirements, etc., are production-worthy

Customer C: Scrub Depth Experiment

- Wafer Setup for Experiment
  - 300mm qual wafer selected in Engineering lab
  - Entire wafer probed with 4 touchdowns on every die
  - Lower 2/3 probed with a 5th touchdown
  - Lower 1/3 probed with a 6th touchdown
- Scrub Mark Review Techniques
  - Center and edge samples collected from each zone
  - Angled photos taken to profile scrub mark shape
  - Passivation cap added to enable FIB cross-sectioning
  - Scrub depth into Aluminum directly measured



Customer C: Scrub Depth Findings

- Pad Scrub Findings
  - Starting aluminum depth of 1.20um
  - Worst-case image: 6 touchdowns at wafer center
  - Aluminum depth of 0.64um shows maximum scrub depth of 0.56um
  - Low scrub was very repeatable across all wafer zones

Conclusions & Use Benefits

- Conclusion
  - The Mx MEMS vertical probe solution addresses key requirements for today's pre-bump probing: low-force, high-accuracy contact, repeatability, and low force. These characteristics can enable effective pre-bump probe for the next generation of pads testing.
- Use Benefits
  - Flows such as eWLP can significantly reduce packaging costs by ensuring only known good die are put into molded carriers & reconstituted wafers
  - Yield learning & improvement can be accelerated by bringing "first look" closer to the wafer fab – no need to wait for bumping to see low yield
  - Long-term quality & reliability of pads-tested devices can be improved by reducing the risk that under-pad circuitry is stressed or damaged

Follow-On Work / Q&A

- Follow-On Work
  - Lifetime testing on accuracy and scrub would be beneficial to understand MEMS stability and repeatability versus legacy solutions
  - Copper pads testing should be conducted – these studies were all done using Aluminum pads
  - Additional hot-temp testing would be useful, as would a cold-temp study
- Questions?

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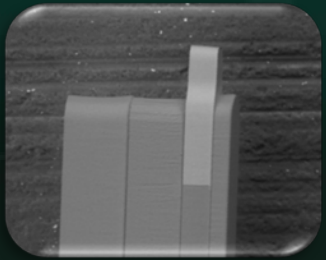

Mx-FP